SUPPLEMENTAL INFORMATION

This Device Errata supplements the information in the data sheet for the IDT79R5000, a multi-issue 64-bit microprocessor.

DESCRIPTIONS and WORKAROUNDS

ITEM #1:

Problem: Any load-linked memory reference that hits in the DTLB will cause the LLAddr register to hold the virtual address of that reference instead of the physical address.

Work-Around: None. This item will not be fixed.

ITEM #2

Problem: If MIPS IV instructions are disabled (C0_Status[31] = 0 and C0_Status[KSU] = UserMode) then it is possible that the 1wxc1, 1dxc1, swxc1 and sdxc1 instructions can cause TLB and Address Error exceptions even though these instructions will not be executed but take FP Unimplemented Exceptions.

Work-Around: None. This item will be fixed in Rev 2 of the device.

ITEM #3:

Problem: C0_CacheErr[2] does not report VirtualAddress [14] of the parity error location. This bit is always read as zero.

Work-Around: None. This item will not be fixed.

ITEM #4:

Problem: An erroneous JTLB miss exception will be taken under these conditions.

a) An instruction which does not cause an exception or stall is 8 bytes away from the end of a page.

b) A load or store instruction is the last instruction of that page.

c) The load/store target address has a matching but invalid JTLB entry

d) The next sequential page is not mapped in the JTLB

In this situation, when the load/store instruction is executed, a JTLB invalid exception should be taken, but instead a JTLB miss exception is incorrectly taken. If the exception handler does a random TLB write to resolve the exception, this will in general insert a duplicate TLB entry for each erroneous exception.

If the first instruction is a jump or branch, this will cause an infinite loop of JTLB miss exceptions to occur upon the return from the exception handler. Otherwise, there will be only one erroneous exception, followed by a correct exception, leaving one duplicate entry in the TLB.

Work-Around: A software fix is for the JTLB miss handler to detect this situation, by probing for a matching TLB entry (treating a hit as being this case), ignore the JTLB miss and treat the exception as an JTLB invalid exception.

This item will be fixed in Rev 2 of the device.

ITEM #5:

Problem: If Any load-linked memory reference that hits in the DTLB will cause the LLAddr register to hold the virtual address of that reference instead of the physical address.

Work-Around: None. This item will not be fixed.

ITEM #6:

Problem: If MIPSIV instructions are disabled (C0_Status[31]=0 and C0_Status[KSU]=UserMode) then it is possible that the lwxc1, ldxc1, swxc1 and sdxc1 instructions can cause TLB and Address Error exceptions even though these instructions will not be executed but take FP Unimplemented Exceptions.

Work-Around: None. This item will be fixed in Rev 2 of the device.

ITEM #7:

Problem: If C0_CacheErr[2] does not report VirtualAddress[14] of the parity error location. This bit is always read as zero.

Work-Around: None. This item will not be fixed.

ITEM #8:

Problem: For the integer multiplier to work correctly, bit 37 of the serial mode stream should be set to logic high. (The first mode bit is bit 0). A circuit problem has been identified in the multiplier.

Work-Around: None. This item will be fixed in Rev 2 of the device.

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ITEM #9:

Problem: If an Icache miss is pending on the SysAD bus and an External Event is issued on the SysAD bus, it's possible that the chip can either report erroneous ITag parity errors or the system might hang. The specific sequence is:

a) The processor is expecting data to return from the system.

b) After the uncompelled release for the processor request, an external agent drives an external write command on the SysAD bus.

c) The processor does an uncompelled release again for the cache miss data. At the same time the external agent starts another external request by asserting ExtRqstB. The external agent again gains ownership of the bus.

d) After a delay the external agent drives an external null command on SysAD to return the bus to the processor

e) The Icache miss data finally arrives on SysAD.

Work-Around: None. This item will be fixed in Rev 2 of the device.

ITEM #10:

Problem: If a bus error occurs on an uncached reference while the L2 cache is enabled, the L2 cache will not perform its tag lookup correctly for the next L2 cache access.

Work-Around: None. This item will be fixed in Rev 2 of the device.

ITEM #11:

Problem: If The chip should take FP Unimplemented exceptions for doing long int to FP conversions where the long integer magnitude is greater than 2^52. There is a set of numbers for which the chip does not take the Unimplemented exception and instead returns an incorrect value.

The numbers that do not take FP Unimplemented exception and will return incorrect values are:

a) For positive numbers where long integer bits [62:52] are all ones. For example:

0x7FFFFFFFFFFFFFFF (+Max) to
0x7FF0000000000000

b) For negative numbers where long integer bits [62:52] are all zeros. For example:

0x8000000000000000 (-Max) to
0x800FFFFFFFFFFFFF

Work-Around: None. This item will be fixed in Rev 2 of the device.