RM7000A vs SR71010A Do not connect pins

RM7000A	SR71010A
Do not Connect	DNC

A5	A05
A7	A07
A11	A11 TriState
A19	A19
B12	B12
B15	B15
C5	C05
C19	TcDCE(2)
D23	TcDCE(3)
E21	TcCWE(2)
E22	TcCWE(3)
H4	H04
W3	W03
Y1	Y01
AA5	AA05
AA10	AA10
AA11	AA11
AA19	AA19
TcClr*	AB15
TcTDE*	AB16
TcDOE*	AC17

Pin Name	Type	Description
RdType	Output	Read Type During the address cycle of a read request, **RdType** indicates whether the read request is an instruction read or a data read.
SysAD[63:0]	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC[7:0]	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the **SysAD** bus during data cycles.
SysCmd[8:0]	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System Command/Data Identifier Bus Parity For the RM7000A, unused on input and zero on output.

Table 18 Clock/Control Interface

Pin Name	Type	Description
SysClock	Input	System clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization
V_{CC}P	Input	**V_{CC}** for PLL Quiet VccInt for the internal phase locked loop. Must be connected to **V_{CC}Int** through a filter circuit.
V_{SS}P	Input	**V_{SS}** for PLL Quiet **V_{SS}** for the internal phase locked loop. Must be connected to **V_{SS}Int** through a filter circuit.

Table 19 Tertiary Cache Interface

Pin Name	Type	Description
TcCLR*	Output	Tertiary Cache Block Clear Requests that all valid bits be cleared in the Tag RAMs. Many RAMs may not support a block clear therefore the block clear capability is not required for the cache to operate.
TcCWE[1:0]*	Output	Tertiary Cache Write Enable Asserted to cause a write to the cache. Two identical signals are provided to balance the capacitive load relative to the remaining cache interface signals.
TcDCE[1:0]*	Output	Tertiary Cache Data RAM Chip Enable When asserted this signal causes the data RAMs to read out their contents. Two identical signals are provided to balance the capacitive load relative to the remaining cache interface signals

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Pin Name	Type	Description
TcDOE*	Input	Tertiary Cache Data RAM Output Enable When asserted this signal causes the data RAMs to drive data onto their I/O pins. This signal is monitored by the processor to determine when to drive the data RAM write enable in a tertiary cache miss refill sequence.
TcLine[17:0]	Output	Tertiary Cache Line Index
TcMatch	Input	Tertiary Cache Tag Match This signal is asserted by the cache Tag RAMs when a match occurs between the value on its data inputs and the contents of the addressed location in the RAM.
TcTCE*	Output	Tertiary Cache Tag RAM Chip Enable When asserted this signal will cause either a probe or a write of the Tag RAMs depending on the state of the Tag RAMs write enable signal. This signal is monitored by the external agent and indicates to it that a tertiary cache access is occurring.
TcTDE*	Output	Tertiary Cache Tag RAM Data Enable When asserted this signal causes the value on the data inputs of the Tag RAM to be latched into the RAM. If a refill of the RAM is necessary, this latched value will be written into the Tag RAM array. Latching the Tag allows a shared address/data bus to be used without incurring a penalty to re-present the Tag during the refill sequence.
TcTOE*	Output	Tertiary Cache Tag RAM Output Enable When asserted this signal causes the Tag RAMs to drive data onto their I/O pins.
TcWord[1:0]	Input/Output	Tertiary Cache Double Word Index Driven by the processor on cache hits and by the external agent on cache miss refills.
TcValid	Input/Output	Tertiary Cache Valid This signal is driven by the processor as appropriate to make a cache line valid or invalid. On Tag read operations the Tag RAM will drive this signal to indicate the line state.

Table 20 Interrupt Interface

Pin Name	Type	Description
INT[9:0]*	Input	Interrupt Ten general processor interrupts, bit-wise ORed with bits 9:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 15 of the interrupt register (bit 6 in R5000 compatibility mode).

Table 21 JTAG Interface

Pin Name	Type	Description
JTDI	Input	JTAG data in JTAG serial data in.

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13 RM7000A Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	V_{CC}IO	A2	V_{SS}IO	A3	V_{SS}IO	A4	TcLine11
A5	Do not connect	A6	V_{SS}IO	A7	Do Not Connect	A8	V_{SS}IO
A9	SysAD32	A10	SysADC1	A11	Do Not Connect	A12	V_{SS}IO
A13	V_{CC}Int	A14	V_{CC}Int	A15	SysAD63	A16	V_{SS}IO
A17	SysAD61	A18	V_{SS}IO	A19	Do Not Connect	A20	TcLine4
A21	V_{SS}IO	A22	V_{SS}IO	A23	V_{CC}IO	B1	V_{SS}Int
B2	V_{CC}IO	B3	V_{SS}Int	B4	V_{SS}IO	B5	TcLine10
B6	SysAD35	B7	SysAD34	B8	V_{CC}Int	B9	SysAD33
B10	SysADC5	B11	SysADC0	B12	Do Not Connect	B13	SysADC7
B14	SysADC6	B15	Do Not Connect	B16	SysAD30	B17	SysAD29
B18	SysAD28	B19	TcLine5	B20	V_{SS}IO	B21	V_{SS}Int
B22	V_{CC}IO	B23	V_{SS}IO	C1	V_{SS}IO	C2	V_{SS}Int
C3	V_{CC}IO	C4	V_{CC}IO	C5	Do Not Connect	C6	TcLine9
C7	SysAD3	C8	SysAD2	C9	V_{CC}Int	C10	SysAD0
C11	SysADC4	C12	V_{CC}Int	C13	SysADC3	C14	SysADC2
C15	SysAD62	C16	V_{CC}Int	C17	SysAD60	C18	TcLine6
C19	Do Not Connect	C20	V_{CC}IO	C21	V_{CC}IO	C22	V_{SS}Int
C23	V_{SS}IO	D1	TcLine13	D2	V_{SS}IO	D3	V_{CC}IO
D4	V_{CC}IO	D5	V_{CC}IO	D6	V_{CC}IO	D7	TcLine8
D8	V_{CC}Int	D9	V_{CC}IO	D10	SysAD1	D11	V_{CC}Int
D12	V_{CC}IO	D13	V_{CC}Int	D14	SysAD31	D15	V_{CC}IO
D16	V_{CC}Int	D17	TcLine7	D18	V_{CC}IO	D19	V_{CC}IO
D20	V_{CC}IO	D21	V_{CC}IO	D22	V_{SS}IO	D23	Do Not Connect
E1	V_{CC}Int	E2	TcLine14	E3	TcLine12	E4	V_{CC}IO
E20	V_{CC}IO	E21	Do Not Connect	E22	Do Not Connect	E23	TcLine1
F1	VssIO	F2	TcLine16	F3	TcLine15	F4	V_{CC}IO
F20	V_{CC}IO	F21	TcLine3	F22	TcLine0	F23	V_{SS}IO
G1	SysAD36	G2	SysAD4	G3	TcLine17	G4	V_{CC}Int
G20	TcLine2	G21	V_{CC}Int	G22	SysAD59	G23	SysAD58
H1	V_{SS}IO	H2	SysAD37	H3	SysAD5	H4	Do Not Connect
H20	V_{CC}Int	H21	SysAD27	H22	SysAD26	H23	V_{SS}IO
J1	SysAD7	J2	SysAD6	J3	V_{CC}Int	J4	V_{CC}IO
J20	V_{CC}IO	J21	V_{CC}Int	J22	SysAD57	J23	SysAD56
K1	SysAD40	K2	SysAD8	K3	SysAD39	K4	SysAD38
K20	SysAD25	K21	SysAD24	K22	SysAD55	K23	SysAD23
L1	SysAD10	L2	SysAD41	L3	SysAD9	L4	V_{CC}Int
L20	V_{CC}Int	L21	SysAD54	L22	SysAD22	L23	SysAD53
M1	V_{SS}IO	M2	SysAD11	M3	SysAD42	M4	V_{CC}IO

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Pin	Function	Pin	Function	Pin	Function	Pin	Function
M20	V_{CC}IO	M21	SysAD52	M22	SysAD21	M23	V_{SS}IO
N1	SysAD43	N2	V_{CC}Int	N3	SysAD12	N4	SysAD44
N20	SysAD19	N21	SysAD51	N22	V_{CC}Int	N23	SysAD20
P1	SysAD13	P2	SysAD45	P3	SysAD14	P4	V_{CC}Int
P20	V_{CC}Int	P21	SysAD49	P22	SysAD18	P23	SysAD50
R1	SysAD46	R2	SysAD15	R3	SysAD47	R4	V_{CC}IO
R20	V_{CC}IO	R21	SysAD16	R22	SysAD48	R23	SysAD17
T1	V_{SS}IO	T2	RspSwap*	T3	PRqst*	T4	V_{CC}Int
T20	ExtRqst*	T21	V_{CC}OK	T22	BigEndian	T23	V_{SS}IO
U1	PAck*	U2	V_{CC}Int	U3	ModeClock	U4	JTCK
U20	V_{CC}Int	U21	NMI*	U22	Reset*	U23	ColdReset*
V1	V_{SS}IO	V2	JTDO	V3	JTMS	V4	V_{CC}IO
V20	V_{CC}IO	V21	INT9*	V22	V_{CC}Int	V23	V_{SS}IO
W1	JTDI	W2	V_{CC}IO	W3	Do Not Connect	W4	V_{CC}IO
W20	V_{CC}IO	W21	INT6*	W22	INT8*	W23	V_{CC}Int
Y1	Do Not Connect	Y2	V_{SS}IO	Y3	V_{CC}IO	Y4	V_{CC}IO
Y5	V_{CC}IO	Y6	V_{CC}IO	Y7	RdRdy*	Y8	Release*
Y9	V_{CC}IO	Y10	TcWord0	Y11	V_{CC}Int	Y12	V_{CC}IO
Y13	SysCmd5	Y14	V_{CC}Int	Y15	V_{CC}IO	Y16	V_{CC}Int
Y17	INT2*	Y18	V_{CC}IO	Y19	V_{CC}IO	Y20	V_{CC}IO
Y21	V_{CC}IO	Y22	V_{SS}IO	Y23	INT7*	AA1	V_{SS}IO
AA2	V_{SS}Int	AA3	V_{CC}IO	AA4	V_{CC}IO	AA5	Do Not Connect
AA6	TcMatch	AA7	ValidOut*	AA8	SysClock	AA9	V_{CC}Int
AA10	Do Not Connect	AA11	Do Not Connect	AA12	SysCmd0	AA13	SysCmd4
AA14	SysCmd8	AA15	TcTCE*	AA16	TcValid	AA17	V_{CC}Int
AA18	INT3*	AA19	Do Not Connect	AA20	V_{CC}IO	AA21	V_{CC}IO
AA22	V_{SS}Int	AA23	V_{SS}IO	AB1	V_{SS}IO	AB2	V_{CC}IO
AB3	V_{SS}Int	AB4	V_{SS}IO	AB5	ModeIn	AB6	Validin*
AB7	VccP	AB8	V_{CC}Int	AB9	V_{CC}Int	AB10	TcCWE0*
AB11	TcDCE0*	AB12	SysCmd1	AB13	SysCmd3	AB14	SysCmd7
AB15	TcClr*	AB16	TcTDE*	AB17	TcDOE*	AB18	INT0*
AB19	INT4*	AB20	V_{SS}IO	AB21	V_{SS}Int	AB22	V_{CC}IO
AB23	V_{SS}Int	AC1	V_{CC}IO	AC2	V_{SS}Int	AC3	V_{SS}IO
AC4	RdType	AC5	WrRdy*	AC6	V_{SS}IO	AC7	V_{SS}P
AC8	V_{SS}IO	AC9	TcWord1	AC10	TcCWE1*	AC11	TcDCE1*
AC12	V_{SS}IO	AC13	SysCmd2	AC14	SysCmd6	AC15	SysCmdP
AC16	V_{SS}IO	AC17	TcTOE*	AC18	V_{SS}IO	AC19	INT1*
AC20	INT5*	AC21	V_{SS}IO	AC22	V_{SS}IO	AC23	V_{CC}IO

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Tertiary Cache Interface Signals

Name	*Definition*	*Direction*	*Reset*	*Description*
TcTCE*	Tertiary Cache Tag SRAM Chip Enable	Output	CR	This signal is monitored by the external agent and indicates to it that a tertiary cache data RAM access is occurring. In SR71010, this signal is only used to indicate a refilling will follow.
TcCWE*[3:0]	Tertiary Cache Data SRAM Write Enable	Output	CR	Two pairs of two identical write enable signals for the tertiary cache are provided to balance loading.
TcDCE*[3:0]	Tertiary Cache Data SRAM Chip Enable	Output	CR	Two pairs of two identical output enable signals for the tertiary cache are provided to balance loading.
TcDOE*	Tertiary Cache Data SRAM Output Enable	Input		This signal comes from the agent and informs the processor that it is beginning or ending its use of the SysAD bus for refilling the tertiary cache.
TcLine[17:0]	Tertiary Cache Sub-block Index	Output	CR	This bus is the index used to access the data RAMs of the tertiary cache.
TcMatch[a]	Tertiary Cache Sub-block Tag Match	Output	CR	The processor asserts this signal whenever a tertiary cache hit is detected to prevent a refill from the agent.
TcWord[1:0]	Tertiary Cache Double Word Index	Input / Output	R	This signal defines the doubleword in a subblock and is driven by the processor on cache hits and by the external agent on cache miss refills.

Notes:

a. If the SR71010 is used in an existing RM7000 system, the tag RAMs must be removed from the board to prevent drive fights on this signal. For the RM7000, TcMatch is an input driven by the external cache controller. For SR71010, with internal tertiary cache tags, the pin is an output used to signal that a hit has occurred in the L3 cache.

Mode ROM Settings

The following table defines the contents of the Mode ROM, which are loaded after a Power-on Reset or Cold Reset sequence.

Bit	*Name*	*Values*			
0	*Reserved*	*Must be 0*			
4:1	*Reserved*[a]	*Must be 0*			
7:5	PClk-to-SClk ratio[b]	*Mode bit 20 = 0*		*Mode bit 20 = 1*	
		000: reserved 001: reserved 010: 4:1 011: 5:1	100: 6:1 101: 7:1 110: 8:1 111: reserved	000: reserved 001: reserved 010: 4.5:1 011: 5.5:1	100: 6.5:1 101: 7.5:1 110: 8.5:1 111: reserved
8	Endian bit (logically Ored with the **BigEndian** pin to define $Config_{BE}$)	0: Little endian ordering 1: Big endian ordering			
14:9	*Reserved*[a]	*Must be 0*			
15	Tertiary data cache SRAM type	0: Dual-cycle deselect 1: Single-cycle deselect			
17:16	*Reserved*[a]	*Must be 0*			
18	Enable extra SR71010 signals[c]	0: RM7000-compatible mode. All do-not-connect pins of RM7000 footprint are truly disconnected on SR71010. Even though the pins are marked as DNC, connections can be made and the SR71010 processor will ignore any signal activity on these lines. The **TcDCE*(3:2)** and **TcCWE*(3:2)** signals are tristated and, internally, the **TriState** pin is deasserted. 1: Extra tertiary cache drivers **TcDCE*(3:2)** and **TcCWE*(3:2)** are enabled, and **TriState** input is enabled. All other do-not-connect pins of customer footprint must be truly disconnected on SR71010[d].			
19	*Reserved*[a]	*Must be 0*			
20	Pclock to SysClock Multipliers[b]	0: Integer (4, 5, 6, 7, 8) 1: Half Integer (4.5, 5.5, 6.5, 7.5, 8.5)			
21	*Reserved*[a]	*Must be 0*			
22	Output drivers slew control[c] (except **TcLine** and **TcWord**)	0: Slow 1: Fast			
23	L3 address drivers slew control[c] (**TcLine** and **TcWord** only)	0: Slow 1: Fast			
255:24	*Reserved*[a]	*Must be 0*			

Table 6: Mode ROM bit definitions

PINOUT AND PACKAGE

The following table gives the pin out for the SR71010 processor. DNC means 'Do Not Connect'.

Pin	*Name*	*Pin*	*Name*	*Pin*	*Name*	*Pin*	*Name*
A01	VccIO	B16	SysAD(30)	D08	VccInt	G22	SysAD(59)
A02	Vss	B17	SysAD(29)	D09	VccIO	G23	SysAD(58)
A03	Vss	B18	SysAD(28)	D10	SysAD(1)	H01	Vss
A04	TcLine(11)	B19	TcLine(5)	D11	VccInt	H02	SysAD(37)
A05	DNC[c]	B20	Vss	D12	VccIO	H03	SysAD(5)
A06	Vss	B21	Vss	D13	VccInt	H04	DNC[c]
A07	DNC[c]	B22	VccIO	D14	SysAD(31)	H20	VccInt
A08	Vss	B23	Vss	D15	VccIO	H21	SysAD(27)
A09	SysAD(32)	C01	Vss	D16	VccInt	H22	SysAD(26)
A10	SysADC(1)	C02	Vss	D17	TcLine(7)	H23	Vss
A11	TriState[b]	C03	VccIO	D18	VccIO	J01	SysAD(7)
A12	Vss	C04	VccIO	D19	VccIO	J02	SysAD(6)
A13	VccInt	C05	DNC[c]	D20	VccIO	J03	VccInt
A14	VccInt	C06	TcLine(9)	D21	VccIO	J04	VccIO
A15	SysAD(63)	C07	SysAD(3)	D22	Vss	J20	VccIO
A16	Vss	C08	SysAD(2)	D23	TcDCE(3) [a]	J21	VccInt
A17	SysAD(61)	C09	VccInt	E01	VccInt	J22	SysAD(57)
A18	Vss	C10	SysAD(0)	E02	TcLine(14)	J23	SysAD(56)
A19	DNC[c]	C11	SysADC(4)	E03	TcLine(12)	K01	SysAD(40)
A20	TcLine(4)	C12	VccInt	E04	VccIO	K02	SysAD(8)
A21	Vss	C13	SysADC(3)	E20	VccIO	K03	SysAD(39)
A22	Vss	C14	SysADC(2)	E21	TcCWE(2) [a]	K04	SysAD(38)
A23	VccIO	C15	SysAD(62)	E22	TcCWE(3) [a]	K20	SysAD(25)
B01	Vss	C16	VccInt	E23	TcLIne(1)	K21	SysAD(24)
B02	VccIO	C17	SysAD(60)	F01	Vss	K22	SysAD(55)
B03	Vss	C18	TcLine(6)	F02	TcLine(16)	K23	SysAD(23)
B04	Vss	C19	TcDCE(2) [a]	F03	TcLine(15)	L01	SysAD(10)
B05	TcLine(10)	C20	VccIO	F04	VccIO	L02	SysAD(41)
B06	SysAD(35)	C21	VccIO	F20	VccIO	L03	SysAD(9)
B07	SysAD(34)	C22	Vss	F21	TcLine(3)	L04	VccInt
B08	VccInt	C23	Vss	F22	TcLine(0)	L20	VccInt
B09	SysAD(33)	D01	TcLine(13)	F23	Vss	L21	SysAD(54)
B10	SysADC(5)	D02	Vss	G01	SysAD(36)	L22	SysAD(22)
B11	SysADC(0)	D03	VccIO	G02	SysAD(4)	L23	SysAD(53)
B12	DNC[c]	D04	VccIO	G03	TcLine(17)	M01	Vss
B13	SysADC(7)	D05	VccIO	G04	VccInt	M02	SysAD(11)
B14	SysADC(6)	D06	VccIO	G20	TcLine(2)	M03	SysAD(42)
B15	DNC[c]	D07	TcLine(8)	G21	VccInt	M04	VccIO

Notes:

a. These output signals are tristated according to bit 18 of the Mode ROM.

b. These inputs will be disconnected and default internally to their deasserted value according to bit 18 of the Mode ROM

c. These signals are *Do-Not-Connect* pins that should not be connected externally.

Pin	Name	Pin	Name	Pin	Name	Pin	Name
M20	VccIO	U03	ModeClock	Y17	Int*(2)	AB09	VccInt
M21	SysAD(52)	U04	JTCK	Y18	VccIO	AB10	TcCWE*(0)
M22	SysAD(21)	U20	VccInt	Y19	VccIO	AB11	TcDCE*(0)
M23	Vss	U21	NMI*	Y20	VccIO	AB12	SysCmd(1)
N01	SysAD(43)	U22	Reset*	Y21	VccIO	AB13	SysCmd(3)
N02	VccInt	U23	ColdReset*	Y22	Vss	AB14	SysCmd(7)
N03	SysAD(12)	V01	Vss	Y23	Int*(7)	AB15	DNC[c]
N04	SysAD(44)	V02	JTDO	AA01	Vss	AB16	DNC[c]
N20	SysAD(19)	V03	JTMS	AA02	Vss	AB17	TcDOE*
N21	SysAD(51)	V04	VccIO	AA03	VccIO	AB18	Int*(0)
N22	VccInt	V20	VccIO	AA04	VccIO	AB19	Int*(4)
N23	SysAD(20)	V21	Int*(9)	AA05	DNC[c]	AB20	Vss
P01	SysAD(13)	V22	VccInt	AA06	TcMatch[d]	AB21	Vss
P02	SysAD(45)	V23	Vss	AA07	ValidOut*	AB22	VccIO
P03	SysAD(14)	W01	JTDI	AA08	SysClock	AB23	Vss
P04	VccInt	W02	VccIO	AA09	VccInt	AC01	VccIO
P20	VccInt	W03	DNC[c]	AA10	DNC[c]	AC02	Vss
P21	SysAD(49)	W04	VccIO	AA11	DNC[c]	AC03	Vss
P22	SysAD(18)	W20	VccIO	AA12	SysCmd(0)	AC04	RdType
P23	SysAD(50)	W21	Int*(6)	AA13	SysCmd(4)	AC05	WrRdy*
R01	SysAD(46)	W22	Int*(8)	AA14	SysCmd(8)	AC06	Vss
R02	SysAD(15)	W23	VccInt	AA15	TcTCE*	AC07	VssP
R03	SysAD(47)	Y01	DNC[c]	AA16	DNC[c]	AC08	Vss
R04	VccIO	Y02	Vss	AA17	VccInt	AC09	TcWord(1)
R20	VccIO	Y03	VccIO	AA18	Int*(3)	AC10	TcCWE*(1)
R21	SysAD(16)	Y04	VccIO	AA19	DNC[c]	AC11	TcDCE*(1)
R22	SysAD(48)	Y05	VccIO	AA20	VccIO	AC12	Vss
R23	SysAD(17)	Y06	VccIO	AA21	VccIO	AC13	SysCmd(2)
T01	Vss	Y07	RdRdy*	AA22	Vss	AC14	SysCmd(6)
T02	RspSwap*	Y08	Release*	AA23	Vss	AC15	SysCmdP
T03	PReq*	Y09	VccIO	AB01	Vss	AC16	Vss
T04	VccInt	Y10	TcWord(0)	AB02	VccIO	AC17	DNC[c]
T20	ExtRqst*	Y11	VccInt	AB03	Vss	AC18	Vss
T21	VccOK	Y12	VccIO	AB04	Vss	AC19	Int*(1)
T22	BigEndian	Y13	SysCmd(5)	AB05	ModeIn	AC20	Int*(5)
T23	Vss	Y14	VccInt	AB06	ValidIn*	AC21	Vss
U01	PAck*	Y15	VccIO	AB07	VccP	AC22	Vss
U02	VccInt	Y16	VccInt	AB08	VccInt	AC23	VccIO

Notes:

c. These signals are *Do-Not-Connect* pins that should not be connected externally.

d. This signal is an input on the RM7000 and is derived from the external tertiary cache tag RAMs. It is used to indicate tertiary cache hits to both the RM7000 and memory controller On SR71010, this signal is an output, due to the internal tertiary cache tag RAMs. It is used to drive the memory controller input.

IMPORTANT NOTE: If the SR71010 is to be used in an existing RM7000 socket, any external tertiary cache RAMs must be removed from the system board to prevent drive fights on this signal.

Table 12: Package Pinout