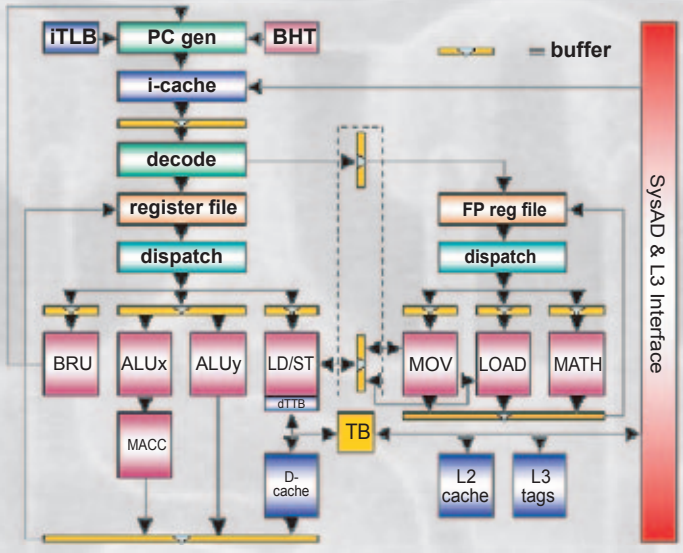
SANDCRAFT
ENGINES FOR THE DIGITAL AGE™

SR71010B
MIPS64™ SUPERSCALAR MICROPROCESSOR

The SR71010B is a true 2-way superscalar MIPS64™ microprocessor with a 9-stage pipeline designed for high performance applications such as networking, image processing and internet servers. The highly efficient architecture can operate up to a maximum frequency of 800MHz, and includes dual instruction fetch, up to 6-issue, up to 6-execute, and dual-commit, to sustain an instruction throughput rate of 2 instructions per cycle. Instruction execution efficiency is maximized for the deep pipeline by including sophisticated branch prediction techniques, that keep the pipeline fully utilized. The SR71010 also maximizes system performance and reduces system cost with integrated on-chip 512 KByte L2 cache, L3 cache controller and L3 cache tags.

The SR71010B has dynamic power management features that minimize power consumption. The high performance system interface, which is fully compatible to R4xxx/5xxx/7xxx SysAD interface, can operate up to 133MHz. The SR71010 includes a high - performance floating point unit (FPU) that is fully IEEE-754™ compliant. The FPU is decoupled from the integer pipeline, enabling autonomous integer and floating point operations.



SR71010B Architecture Block Diagram

High performance architecture
- Fully MIPS64 Instruction Set Architecture (ISA) compliant

True 2-way superscalar architecture
- Dual fetch, dual dispatch, up to 6-issue, up to 6-execute, dual-commit
- Maximum operation rate of pipeline: 2 instructions per cycle
- Out-of-order issue and dispatch
- In-order retires

9-stage pipeline for high clock frequency
- Optimized pipeline bypass architecture for minimizing instruction interdependent stalls

Intelligent dynamic branch prediction
- Bi-modal 3Kbit table, Branch predictor
- Keeps pipeline full and minimizes branch mis-predict penalties
- Speculative execution down predicted paths maximizes sustainable performance

Low power consumption
- Clock enabled registers for improved power management
- Dynamic activation of sense amps. in caches

High-performance system interface
- Compatible with R4xxx/5xxx/7xxx
- SysAD interface133 MHz

High-performance floating point
- Fully MIPS64 compliant
- IEEE - 754 compatible
- Decoupled from Integer pipeline

Extended features
- 10 interrupts
- 64 dual-entry TLB
- Variable page sizes from 4 KBytes to 256 MBytes
- JTAG interface compatible with IEEE 1149.1

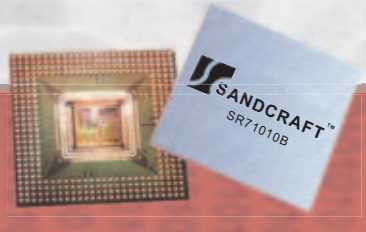
Cache Hierarchy

Primary Instruction Cache - (L1)
- 32 KB, 32 byte line
- 4-way set associative
- Line Locking

Primary Data Cache - (L1)
- 32 KB, 32 byte line
- 4-way set associative
- Line Locking
- Write Back, Write Through (Write-Allocate/No-Write-Allocate), Bypass L2-L3

Secondary Unified Cache - (L2)
- 512 KB on chip
- 8-way set associative
- 32-byte line, line locking

Tertiary cache - (L3)
- On-chip tag RAMs supporting:
- 2, 4, 8, or 16 MB external cache
- 8-way set associative
- 32 byte line, line locking



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SR71010B

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SR71010B - 600-800 MHz

Core frequency	600MHz - 800 MHz		
Instruction cache	32 KByte	Interface bus width (MIPS SysAD)	64-bit
Data cache	32 KByte	Interface bus frequency	Up to 133 MHz
L2 cache	512 KByte	Process	0.13um
L3 cache	Up to 16 MByte	Core VCC	1.2V - 1.4V
Package	256 & 304 TBGA	I/O VCC	2.5V or 3.3V

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- SR71010B: SandCraft Designator
- XXX: CPU Speed
- 3: Package Size
- Y: Package Type

PART NUMBER	CPU FREQUENCY MHz	PACKAGE	L2	L3
SR71010B	800, 700, 600	304 TBGA	512 KB, 8-way set associative	2,4,8, or 16 MByte
SR71000B	800, 700, 600	304 TBGA	512 KB, 8-way set associative	
SR71012B	800, 700, 600	256 TBGA	512 KB, 8-way set associative	

DEVELOPMENT TOOLS

Compilers:	RedHat (Cygnus)
Operating systems:	Wind River: Vxworks, RedHat: Linux
Simulation tools:	SandCraft
Development boards:	SandCraft, Marvell

APPLICATIONS

Internet:
- Storage servers
- Web servers

Image Processing:
- Copiers
- Printers

Networking:
- Access
- Routers
- Switches

Workstations

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