IBM PowerPC 970MP RISC Microprocessor Datasheet

Version 1.3

January 17, 2008

Printed in the United States of America January 2008

IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

The IBM home page can be found at **ibm.com®**

The IBM semiconductor solutions home page can be found at **ibm.com**/chips

January 17, 2008

Contents

List of Figures

List of Tables

Revision Log

Revision	Modification
January 17, 2008	Version 1.3 • Changed the tolerance associated with the I/O supply voltage and added a footnote explaining that OV_{DD} cannot exceed V0 by more than 0.8 V (see *Table 3-3 Recommended Operating Conditions* on page 24).
July 19, 2007	Version 1.2 • Updated the power values and removed the integer only column in *Table 3-6 Power Consumption* on page 26. • Updated the TCK frequency of operation minimum value in *Table 3-24 JTAG ac Timing Specifications (Dependent on SYSCLK)* on page 42.
March 29, 2007	Version 1.1 • Removed the power-optimized part information. • Updated product offering part numbers in *Table 1-1 PowerPC 970MP Ordering and Processor Version Register* on page 18. • Updated *Figure 1-3 Part Number Legend* on page 19. • Provided a value for the storage temperature range (see *Table 3-1 Absolute Maximum Ratings* on page 23). • Updated *Table 3-6 Power Consumption* on page 26. • Updated *Table 3-7 PowerPC 970MP V0 and V1 V_{DD}* on page 26. • Provided the V_{DD} tolerance (see *Table 3-7 PowerPC 970MP V0 and V1 V_{DD}* on page 26). • Removed a note about disabling on-chip termination from *Figure 3-3 Block Diagram of an SSB for a PowerPC 970MP Processor Interconnect Implementation* on page 30. • Corrected the total skew value (see *Section 3.5.1.4 Receive Side Characteristics* on page 32). • Provided pull-up resistor values (see *Table 3-19 Asynchronous Open-Drain Output Signals* on page 36 and *Table 3-20 Asynchronous Open-Drain Bidirectional Signals* on page 36). • Changed the description of the GPULDBG pin (see *Table 3-23 Debug Pins* on page 39). • Revised the comments about the $\overline{\text{TRST}}$ signal (see *Table 5-7 PowerPC 970MP Debug and Bringup Pin Settings and Information* on page 64). • Revised the description of thermal management (see *Section 5.8* on page 70).
July 31, 2006	Version 1.0 • Declassified for general availability. • Updated power and part number tables.

About This Datasheet

This datasheet describes the IBM PowerPC® 970MP RISC Microprocessor. This microprocessor, also called the PowerPC 970MP, is a dual core, 64-bit implementation of the IBM PowerPC family of reduced instruction set computer (RISC) microprocessors that are based on the PowerPC Architecture™.

Who Should Read This Datasheet

This datasheet is intended for designers who plan to develop products using the PowerPC 970MP.

Related Publications

Related IBM publications include the following:

- *PowerPC 970MP RISC Microprocessor User's Manual*
- *PowerPC 970MP Power-On Reset Application Note*
- *PowerPC 970MP DD1.x Errata List*

Note: Subscribe to PowerPC at the IBM Customer Connect Web site or contact your IBM representative to verify that you have the latest version of the publication.

https://www-309.ibm.com/technologyconnect/

Other related publications include the following:

The I^2C-bus specification. This document can be downloaded from the NXP web site at http://www.nxp.com/products/interface_control/i2

Conventions and Notations Used in This Datasheet

The use of overbars designates signals that are active low or the complement of differential signals. For example, $\overline{\text{DDEL\_OUT}}$.

The following software documentation conventions are used in this manual:

1. Function names are written in **bold** type. For example, **np_npms_proc_register ()**.
2. Variables are written in italic type. For example, *enable_mode*.
3. Keywords and data types are written all in capitals with underlines between words. For example, OFF_DISABLED.

1. General Information

1.1 Description

The IBM PowerPC 970MP RISC Microprocessor is a dual-core, 64-bit implementation of the IBM PowerPC family of reduced instruction set computer (RISC) microprocessors that are based on the PowerPC Architecture. This dual microprocessor, also called the PowerPC 970MP, includes a vector/single instruction, multiple data (SIMD) facility that supports high-bandwidth data processing and compute-intensive operations. The PowerPC 970MP is also designed to support multiple system organizations, including desktop and low-end server applications, up through 4-way symmetric multiprocessor (SMP) configurations.

Note: The IBM PowerPC 970MP incorporates two complete microprocessors on a single chip, along with some common logic to connect these microprocessors to a system. The terms microprocessor, processor, and processing unit (PU) are used interchangeably to describe each of the two individual processors. The term core refers to the instruction fetch and execution logic, including the level 1 (L1) caches, but excluding the storage subsystem, of each processor.

Figure 1-1 on page 16 is a block diagram of a single PowerPC 970MP processor, indicating the main functional units of the core and the storage subsystem (STS).

Figure 1-2 on page 17 is a block diagram of the entire PowerPC 970MP design, showing how the two processing units (PU0 and PU1) are connected through the common logic to the processor interface.

This document also provides pertinent physical characteristics of the PowerPC 970MP module.

1.2 Processor Features

- 64-bit implementation of the PowerPC Architecture Specification (version 2.0)
  - Binary compatibility for all PowerPC application level code (problem state)
  - Support for the 32-bit bridge facility
  - Vector/SIMD multimedia extension unit
- Layered implementation strategy for very-high-frequency operation
  - Deeply pipelined design
    - 16 stages for most fixed-point register-to-register operations
    - 18 stages for most load and store operations (assuming an L1 data cache hit)
    - 21 stages for most floating-point operations
    - 19 stages for fixed-point, 22 stages for complex-fixed, and 25 stages for floating-point operations in the vector arithmetic logic unit (VALU)
    - 19 stages for vector/SIMD multimedia extension permute operations
- Dynamic instruction cracking for some instructions allows for simpler inner core dataflow
  - Dedicated dataflow for cracking one instruction into two internal operations
  - Microcoded templates for longer emulation sequences
- Speculative superscalar inner core organization
  - Aggressive branch prediction
    - Prediction for up to two branches per cycle
    - Support for up to 16 predicted branches in flight
    - Prediction support for branch direction and branch addresses
  - In-order dispatch of up to five operations into the distributed issue queue structure

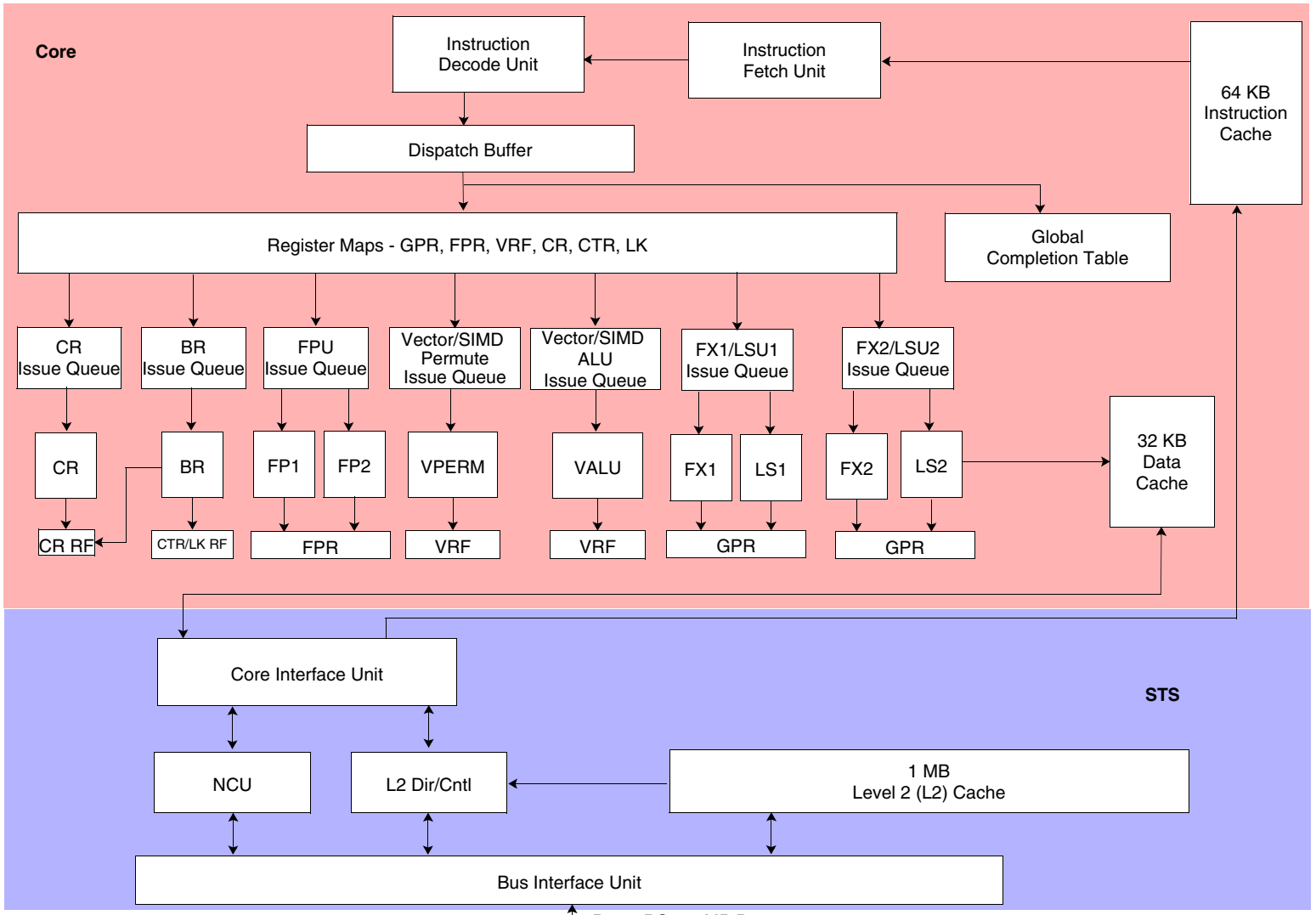
  - Out-of-order issue of up to 10 operations into 10 execution pipelines
    - Two load or store operations
    - Two fixed-point register-to-register operations
    - Two floating-point operations
    - One branch operation
    - One Condition Register operation
    - One vector/SIMD multimedia extension permute operation
    - One vector/SIMD multimedia extension arithmetic logic (ALU) operation
  - Register renaming on general purpose registers (GPRs), floating-point registers (FPRs), vector register files (VRFs), Condition Register (CR) fields, Integer Exception Register (XER), Floating-Point Status and Control Register (FPSCR), Vector Status and Control Register (VSCR), Vector Register Save (VRSAVE), and Link and Count
- Large number of instructions in flight (theoretical maximum of 215 instructions)
  - Up to 16 instructions in the instruction fetch unit (fetch buffer and overflow buffer)
  - Up to 32 instructions in the instruction fetch buffer in the instruction decode unit
  - Up to 35 instructions in the three decode pipe stages and four dispatch buffers
  - Up to 100 instructions in the inner core (after dispatch)
  - Up to 32 stores queued in the store queue (STQ) (available for forwarding)
- Fast, selective flush of incorrect speculative instructions and results
- Specific focus on storage latency management
  - Out-of-order and speculative issue of load operations
  - Support for up to eight outstanding L1 cache line misses
  - Hardware-initiated instruction prefetching from the level 2 (L2) cache
  - Software-initiated data stream prefetching
    - Support for up to eight active streams
  - Critical word forwarding; critical sector first
  - Prediction hints on branch instructions
- Power management
  - Static power management
    - Software initiated doze, nap, and deep nap modes
  - Dynamic power management
    - Parts of the design stop their (hardware-initiated) clocks when not in use
  - Power tuning engine
    - Software-initiated slow down of the processor; selectable to a half or a quarter of the nominal operating frequency
    - Programmable latency for power mode transitions to control current spikes

1.3 PowerPC 970MP Module Features

- Dual processors on a single chip
  - Each processor has its own dedicated storage subsystem, including a 1 MB L2 cache per core.
  - Each processor has its own dedicated resets, external interrupt, thermal diode, and voltage plane (common logic is powered on).
  - Common logic provides arbitration for bus access between the two cores.
  - A single external interface allows a companion chip with a single interface to support two processors.
- Processor interface (PI) that supports bus speeds up to 1066 MHz
- Pervasive logic supports fencing off one processor for fault isolation or power management.

1.4 PowerPC 970MP Processing Unit Block Diagram

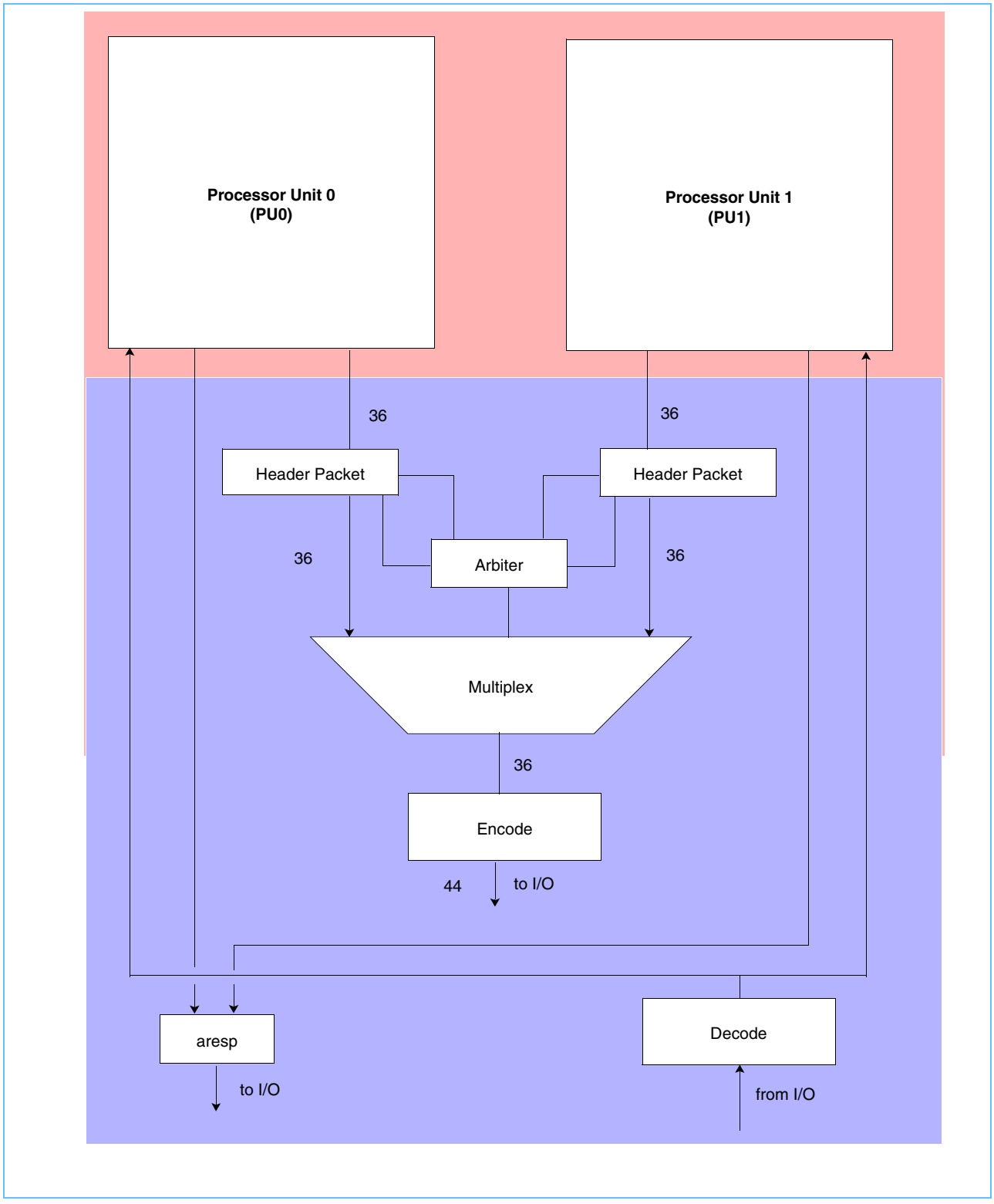
Figure 1-1. PowerPC 970MP Processing Unit Block Diagram



ALU	Arithmetic logic unit	FPR	Floating-point register	LSU	Local store unit	VALU	Vector arithmetic logic uni
BR	Branch	FPU	Floating-point unit	NCU	Noncacheable unit	VPERM	Vector permute unit
CR	Condition Register	FX	Fixed point	RF	Register file	VRF	Vector register file
CTR	Counter Register	GPR	General purpose register	SIMD	Single-instruction, multiple-data		
FP	Floating point	LK	Link bit	STS	Storage subsystem		

1.5 PowerPC 970MP Dual Core with Common Arbitration Logic

Figure 1-2. PowerPC 970MP Dual Core with Common Arbitration Logic



1.6 Ordering Information

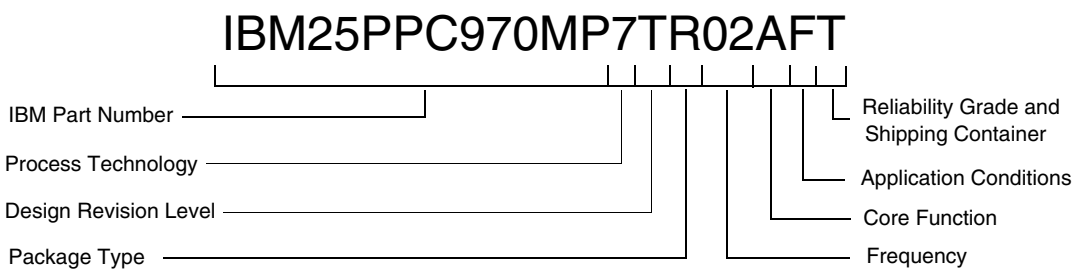
Table 1-1 lists the PowerPC 970MP part numbers and Processor Version Register (PVR) values for the respective design revision levels. See *Figure 1-3* on page 19 for the part number legend.

Table 1-1. PowerPC 970MP Ordering and Processor Version Register

Order Part Number	Frequency (GHz)	Revision Level	PVR
IBM25PPC970MP7TR02AFT	1.2	DD1.1x	x‘00440101’
IBM25PPC970MP7TR06AFT	1.4		
IBM25PPC970MP7TR21AFT	1.6		
IBM25PPC970MP7TR25AFT	1.8		
IBM25PPC970MP7TR31AFT	2.0		

Note: See *Table 3-6 Power Consumption* on page 26 for power and *Table 3-7 PowerPC 970MP V0 and V1 V_{DD}* on page 26 for voltage ratings.

Figure 1-3. Part Number Legend



Process Technology	7 = 10KE
Design Revision Level	T = DD1.12
Package Type	R = Reduced-lead ceramic ball grid array with 576 balls
Frequency	02 = 1.2 GHz 06 = 1.4 GHz 21 = 1.6 GHz 25 = 1.8 GHz 31 = 2.0 GHz
Core Function	A = Dual core
Application Conditions	F = 105°C, V_{DD}±25 mV
Reliability Grade and Shipping Container	T = Grade 3 reliability, tray. Note 1: Automatic array recovery must be enabled as detailed in the *PowerPC 970MP Power-On Reset Application Note*. Note 2: Grade 3 is 100 failures in time (FIT) average failure rate (AFR) at 60°C for 40K and 100K power-on hours (POH).

2. General Parameters

Table 2-1 summarizes the general parameters of the PowerPC 970MP.

Table 2-1. General Parameters of the PowerPC 970MP

Item	Description	Notes
Maximum Die Size	153.8 mm^2	
Maximum Die Dimensions	13.225 mm × 11.629 mm	
Transistor Count	183 million	1
Package	575-pin ceramic ball grid array (CBGA), 25 x 25 mm (1.0 mm pitch)	

Note:

1. For information only. Use of this value to calculate reliability is not valid.

3. Electrical and Thermal Characteristics

This section provides both alternating current (ac) and direct current (dc) electrical specifications and thermal characteristics for the PowerPC 970MP.

3.1 dc Electrical Characteristics

The tables in this section describe the PowerPC 970MP dc electrical characteristics.

3.1.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit	Notes
Core supply voltages	V0, V1 (V_{DD})	-0.3 to 1.5	V	1, 2
I/O supply voltage	V2 (OV_{DD})	-0.3 to 1.7	V	1, 2
Phase-locked loop (PLL) supply voltage	AV_{DD}	-0.3 to 3.0	V	1, 2
Input voltage	V_{IN}	-0.3 to 1.7	V	1, 3
Storage temperature range	T_{STG}	-40 to 125	°C	1

Note:

1. *Table 3-3* on page 24 provides functional and tested operating conditions for OV_{DD}, AVDD, and V_{IN}. *Table 3-7* on page 26 for provides functional and tested operating conditions V0 and V1. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above might affect device reliability or cause permanent damage to the device.
2. Power supply ramping recommendations:
   The order does not matter as long as the supplies reach their final destination in 2 s.
   V0 cannot exceed OV_{DD} by more than 0.8 V (Except for 2 s during power up or down, where it is allowed to be ≤ 1.55 V).
   OV_{DD} cannot exceed V0 by more than 0.8 V (Except for 2 s during power up or down, where it is allowed to be ≤ 1.5 V).
   AV_{DD} cannot exceed V0 by more than 2.5 V (Except for 2 s during power up or down, where it is allowed to be ≤.2.75 V).
   The V1 circuitry is independent of V0, AV_{DD}, and OV_{DD}.
3. This is an implied dc voltage specification. Pending further evaluation, an allowance for ac overshoot or undershoot might be accommodated beyond this input voltage specification.

Table 3-2. Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)

Pin Name	Package Location	Maximum Current
CP0_KELV_GND0	W2	2.7 mA
CP1_KELV_GND1	W22	2.7 mA
CP0_KELV_V0	AB4	2.7 mA
CP1_KELV_V1	W21	2.7 mA
KELV_OV_{DD}	A10	13 mA
KELV_GND2	B13	13 mA

3.1.2 Recommended Operating Conditions

Table 3-3. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
PLL supply voltage[1]	AV_{DD}	2.70±50 mV	V
PLL supply current, maximum	AI_{DD}	20	mA
I/O supply voltage[2]	OV_{DD}	1.5±25 mV	V
I/O supply current, maximum[3]	OI_{DD}	2	A
Input voltage	V_{IN}	GND to OV_{DD}	V
Thermal diode temperature	T_{DIODE}	0 to 105	°C

Notes:

1. The PLL supply voltage has been adjusted to account for the maximum possible dc drop across the filter circuit. See *Section 5.3 PLL Power Supply Filtering* on page 60.
2. OV_{DD} cannot exceed V0 by more than 0.8 V (Except for 2 s during power up or down, where it is allowed to be ≤ 1.5 V).
3. The I/O supply current is for regulator sizing and power distribution information only. The I/O power for thermal design is included in *Table 3-6 Power Consumption* on page 26.

Note: These values are preliminary and subject to change after characterization.

3.1.3 Package Thermal Characteristics

Table 3-4. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
Ceramic ball grid array (CBGA) thermal conductance from junction to board	θ_{JB}	5.4	°C/W

3.1.4 dc Electrical Specifications

Table 3-5. dc Electrical Specifications

Characteristic	Symbol	Voltage		Unit	Notes
		Minimum	Maximum		
SYSCLK, $\overline{\text{SYSCLK}}$ input high voltage	—	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	1
SYSCLK, $\overline{\text{SYSCLK}}$ input low voltage	—	-0.3	$0.3 \times OV_{DD}$	V	1
Processor interface (PI) input high voltage	V_{IH}	$(0.5 \times OV_{DD}) + 0.2$	—	V	2
PI input low voltage	V_{IL}	—	$(0.5 \times OV_{DD}) - 0.2$	V	2
NonPI input high voltage	V_{IH}	$0.7 \times OV_{DD}$	—	V	3
NonPI input low voltage	V_{IL}	—	$0.3 \times OV_{DD}$	V	3
PI output high voltage	V_{OH}	$0.78 \times OV_{DD}$	—	V	4
PI output low voltage	V_{OL}	—	$0.22 \times OV_{DD}$	V	4
NonPI output high voltage, I_{OH} = -2 mA	V_{OH}	$OV_{DD} - 0.2$	—	V	—
NonPI output low voltage, I_{OL} = 2 mA	V_{OL}	—	0.2	V	—
Open-drain (OD) output low, I_{OL} = 2 mA (CHKSTOP, I2CGO)	V_{OL}	—	0.2	V	5
OD output low, I_{OL} = 5 mA (I^2C)	V_{OL}	—	0.2	V	—
Input leakage current, $V_{IN} = OV_{DD}$ and V_{IN} = 0 V	II_N	—	60	µA	—
Hi-Z (off state) leakage current, $V_{OUT} = OV_{DD}$ and V_{OUT} = 0 V	I_{TSO}	—	60	µA	—
Input capacitance, V_{IN} = 0 V, f = 1 MHz	C_{IN}	—	5.0	pF	6

Notes:

1. The SYSCLK differential receiver requires a high-speed transceiver logic (HSTL) differential signaling level. See the Joint Electron Device Engineering Council (JEDEC) HSTL standard.
2. See *Section 3.5 Processor Interconnect Specifications* on page 30. Minimum input must meet the eye opening requirements of the link.
3. The Joint Test Action Group (JTAG) signals TDI, TMS, and $\overline{\text{TRST}}$ do not have internal pullups; therefore, a pullup must be added to the system board. Pullups should be added and adjusted according to the system implementation. These input and outputs meet the dc specification in the JEDEC standard JESD8-11 for the 1.5 V normal power supply range.
4. A 100 Ω split terminator is the test load. Note that a 40 Ω driver has an up level of $0.78 \times OV_{DD}$ for V_{OH} and $0.22 \times OV_{DD}$ at V_{OL}. See *Section 3.5 Processor Interconnect Specifications* on page 30 for information about other drivers.
5. There are two open-drain signals that use this type of driver: CHKSTOP and I2CGO. The pullup for these nets depends on the rise time requirement, net load, and topology. The following examples are two bounding suggestions based on a point-to-point 50 Ω net with two lengths (5 cm and 61 cm). A 33 Ω series source terminator was added in both runs.

   Examples:
   500 Ω pullup dc low level 0.18 V at the receiver
   T_{rise} 0.2 V - 0.8 V = 55 ns at 61 cm
   T_{rise} 0.2 V - 0.8 V = 10 ns at 5 cm

   1 kΩ pullup dc low level 0.13 V at the receiver
   T_{rise} 0.2 V - 0.8 V = 115 ns at 61 cm
   T_{rise} 0.2 V - 0.8 V = 20 ns at 5 cm
6. Capacitance values are guaranteed by design and characterization, and are not tested.

3.1.5 Power Consumption

3.1.5.1 Power Table

Table 3-6. Power Consumption

Frequency	Condition	Voltage	Power (W)	Doze Power (W)	Nap Power (W)	Notes
1.2 GHz	Typical average at 65°C	See *Table 3-7*	32	18	13	2
	Maximum at 105°C		50	36	31	1, 2
1.4 GHz	Typical average at 65°C	See *Table 3-7*	38	20	14	2
	Maximum at 105°C		60	41	35	1, 2
1.6 GHz	Typical average at 65°C	See *Table 3-7*	39	22	15	2
	Maximum at 105°C		65	46	40	1, 2
1.8 GHz	Typical average at 65°C	See *Table 3-7*	47	27	18	2
	Maximum at 105°C		75	52	44	1, 2
2.0 GHz	Typical average at 65°C	See *Table 3-7*	59	33	22	2
	Maximum at 105°C		100	72	61	1, 2

1. Maximum power is projected at the nominal V_{DD} worst case I_{DDq}, and maximum temperature as specified.
2. Voltage tolerance is per the V_{DD} fuse code (VFC). See *Table 3-7 PowerPC 970MP V0 and V1 V_{DD}*.

3.1.5.2 Voltage Table

V0 and V1 voltage information for the 970MP is stored in the fuse ring of each core of the microprocessor using a 3-bit code, with one parity bit. This information should be read for core 0 and the board voltages set appropriately. See *Section 5.9.1 VFC Fusing Implementation* on page 72 for more information.

Table 3-7. PowerPC 970MP V0 and V1 V_{DD}

V_{DD} Fuse Code, Parity	1.2 GHz	1.4 GHz	1.6 GHz	1.8 GHz	2.0 GHz
	V0 and V1 ±25 mV	V0 and V1 ±25 mV	V0 and V1 ±25 mV	V0 and V1 ±25 mV	V0 and V1 ±25 mV
001,1	0.950 V	0.950 V	0.950 V	0.950 V	1.050 V
010,1	0.975 V	0.975 V	0.975 V	0.975 V	1.075 V
011,0	1.000 V	1.000 V	1.000 V	1.000 V	1.100 V
100,1	1.025 V	1.025 V	1.025 V	1.025 V	1.125 V
101,0	1.050 V	1.050 V	1.050 V	1.050 V	1.150 V
110,0	1.075 V	1.075 V	1.075 V	1.075 V	1.175 V
111,1	1.100 V	1.100 V	1.100 V	1.100 V	1.200 V

Notes:

1. Voltage and tolerance should be measured at CP0_KELV_V0 and CP0_KELV_GND0 for V_{DD}Core0; it should be measured at CP1_KELV_V1 and CP1_KELV_GND1 for V_{DD}Core1. Most applications should expect an offset between these Kelvin pins and the voltage and ground planes of the printed circuit board (PCB). This offset is design dependent and should be verified by characterization
2. The entry for 111,1 should be used as the booting voltage. See *Section 5.9.2 Booting Voltage* on page 72.

3.2 ac Electrical Characteristics

This section provides the ac electrical characteristics for the PowerPC 970MP. After fabrication, parts are sorted by maximum processor core frequency as shown in *Section 3.3 Clock ac Specifications*, and they are tested for conformance to the ac and dc specifications for that frequency. The processor core frequency is determined by the SYSCLK and by the settings of the PLL_MULT signal.

This section only describes asynchronous and mode-select inputs and outputs. For bus timing information, see *Section 3.5 Processor Interconnect Specifications* on page 30.

3.3 Clock ac Specifications

Table 3-8 provides the clock ac timing specifications as defined in *Figure 3-1 Clock Differential HSTL Signal* on page 28.

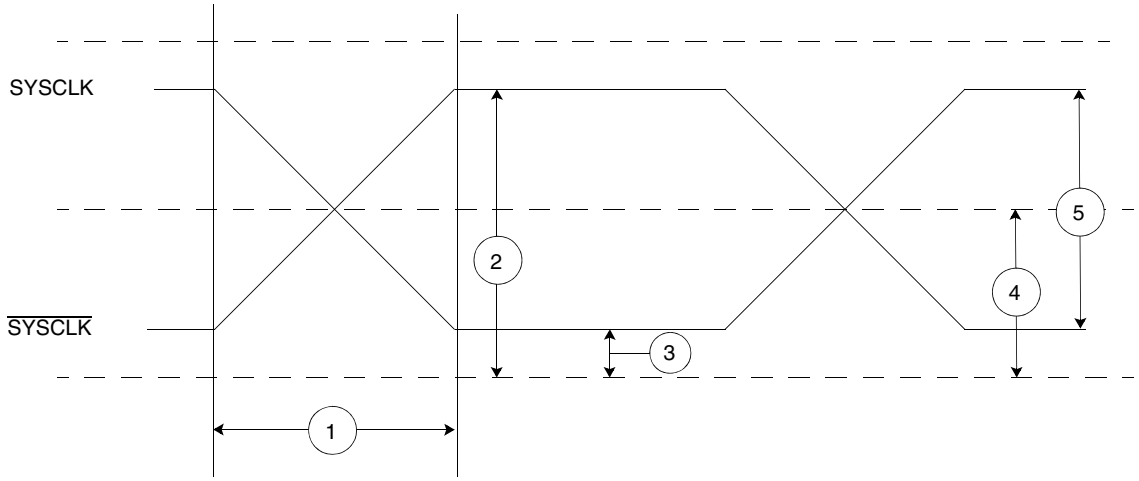
Table 3-8. Clock ac Timing Specifications

Callout Number	Characteristic	Value		Unit	Notes
		Minimum	Maximum		
—	SYSCLK frequency	100	700	MHz	1, 2, 3, 4
—	SYSCLK input jitter (cycle-to-cycle period jitter)	—	±75	ps	3
1	SYSCLK rise and fall time	—	500	ps	5, 3, 6
2	SYSCLK and $\overline{\text{SYSCLK}}$ input high voltage	—	OV_{DD} + 0.3	V	3, 6
3	SYSCLK and $\overline{\text{SYSCLK}}$ input low voltage	-0.3	—	V	3, 6
4	Differential crossing point voltage	0.4 × OV_{DD}	0.6 × OV_{DD}	V	3, 6
5	Differential voltage absolute value | SYSCLK - $\overline{\text{SYSCLK}}$) |	0.385	1.6	V	3, 7, 6
—	PLL lock time	—	800	µs	3, 8
—	Duty cycle	40%	60%	—	—

Notes:

1. **Important:** Processor frequency is determined by PLL_MULT and SYSCLK input frequency. PLL_RANGE(1:0) must be set to the correct values for the expected processor frequency. See *Table 5-2 PowerPC 970MP PLL Configuration* on page 59 for the allowable frequency range for these pins. **Caution:** The PLL_MULT and PLL_RANGE bits can be overwritten by JTAG commands (that is, in test mode) during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
2. The PowerPC 970MP minimum processor frequency is determined by characterization. The minimum frequency is an estimate.
3. **Important:** The data in this table is based on simulation and might be revised after hardware characterization.
4. SYSCLK minimum frequency is for PLL mode. In PLL bypass mode ($\overline{\text{BYPASS}}$ low), SYSCLK frequency can be as low as 10 MHz when not in functional mode (that is, while reading the fuse ring).
5. Rise and fall times for the SYSCLK inputs are measured from 0.4 to 1.0 V.
6. For a timing diagram, see *Figure 3-1 Clock Differential HSTL Signal* on page 28.
7. The differential voltage is the minimum peak-to-peak voltage on both the SYSCLK and $\overline{\text{SYSCLK}}$ pins (similar to what would be measured with single-ended oscilloscope probes).
8. Guaranteed by design and not tested.

Figure 3-1. Clock Differential HSTL Signal



Note: The legend for this figure is provided in *Table 3-8 Clock ac Timing Specifications* on page 27.

To determine the core clock, multiply the SYSCLK by one of the following:

- 12 for PLL_MULT = '0'
- 8 for PLL_MULT = '1'

For more information about the PLL configuration, see *Table 5-2 PowerPC 970MP PLL Configuration* on page 59.

3.4 Core-Clock Timing Relationship between PSYNC and SYSCLK

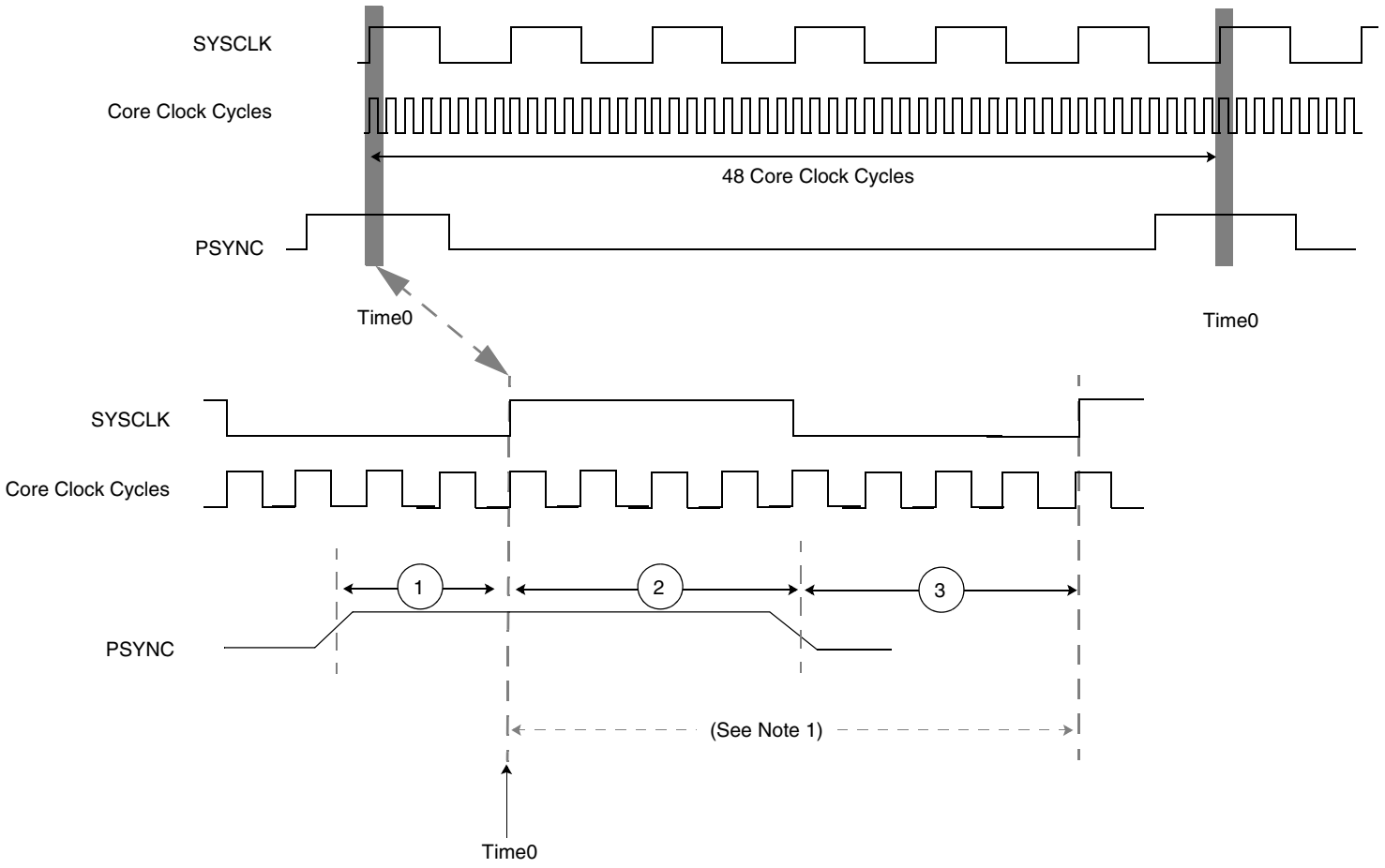
Table 3-9 and *Figure 3-2 Core-Clock Timing Relationship Between PSYNC and SYSCLK* on page 29 provide a description of the core-clock timing relationship between PSYNC and SYSCLK.

Table 3-9. Core-Clock Timing Relationship Between PSYNC and SYSCLK

Callout Number	Characteristic		Value		Unit
			Minimum	Maximum	
1	Setup time	t_{SETUP}	600	—	ps
2	Hold time	t_{HOLD}	100	—	ps
3	Guard time	t_{GUARD}	600	—	ps

Note: See *Figure 3-2 Core-Clock Timing Relationship Between PSYNC and SYSCLK* on page 29 for the corresponding timing diagram.

Figure 3-2. Core-Clock Timing Relationship Between PSYNC and SYSCLK



Notes:

1. A maximum of 48 core-clock cycles between PSYNCs is allowed, independent of the PLL multiplier. One pulse per 24 SYSCLKs is suggested.
2. The legend for this figure is provided by callout number in *Table 3-9 Core-Clock Timing Relationship Between PSYNC and SYSCLK* on page 28.

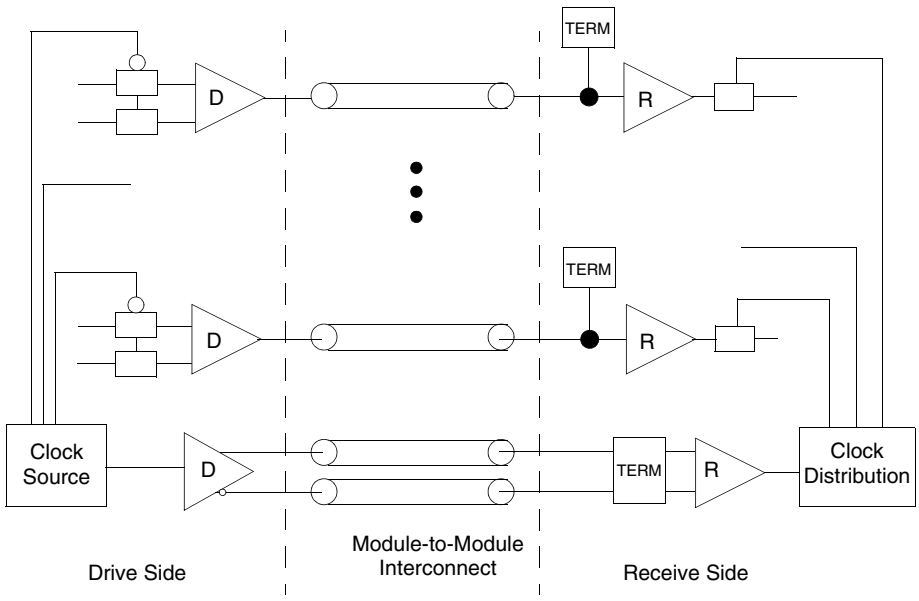
3.5 Processor Interconnect Specifications

3.5.1 Electrical and Physical Specifications

3.5.1.1 Source Synchronous Bus

Figure 3-3 provides a representative block diagram of a source synchronous bus (SSB) for a PowerPC 970MP processor interconnect implementation. Each SSB consists of three major subsections: the drive side, the module-to-module interconnect, and the receive side. Data is first either balance-coding-method (BCM) encoded or checksummed; then it is clock-phase multiplexed; and finally it is launched from the drive side onto the module-to-module interconnect. The receive side includes far-end termination and circuitry to demultiplex and deskew data, align clocks, and synchronize the received data.

Figure 3-3. Block Diagram of an SSB for a PowerPC 970MP Processor Interconnect Implementation



3.5.1.2 Drive Side Characteristics

Figure 3-4 on page 31 shows a typical implementation for a single-ended line. The drivers are of the push-pull type with a nominal impedance (R0 of 20 Ω) that overdrives the line impedance. The nominal swing at the receiver, terminated with resistance (TR0 of 110 Ω) to each rail, is 13% OV_{DD} to 87% OV_{DD}. R0 is 20 Ω when the driver is in the low output impedance mode. The 20 Ω setting is suitable for all bus speeds. The PowerPC 970MP has a 40 Ω nominal output impedance mode that is suitable for bus speeds below 800 megatransfers per second (MTps) in some applications.

The maximum skew between any of the outputs is 150 ps at the ball grid array (BGA) pin. The maximum interconnect skew on the processor cards between any two outputs must be less than 150 ps. The interconnect skew on the processor cards between any two inputs must be less than 300 ps.

Figure 3-4. Typical Implementation for a Single-Ended Line

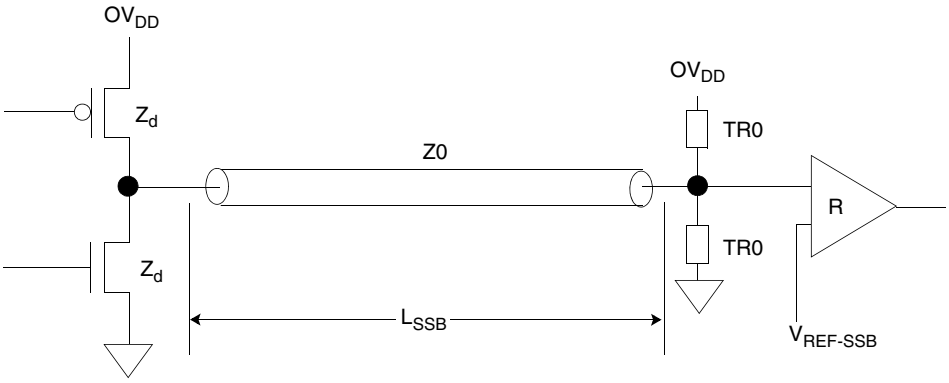


Table 3-10. Processor Interconnect SSB Driver Specifications

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
V_{OHdc}	High output level at dc	—	0.87 OV_{DD}	—	mV	
V_{OLdc}	Low output level at dc	—	0.13 OV_{DD}	—	mV	
T_{DR}	Driver rise time	70	133	171	ps	20% to 80% of swing
T_{DF}	Driver fall time	81	155	162	ps	20% to 80% of swing
Z_D	Driver output impedance	15	20	25	Ω	Low-Ω mode
Z_D	Driver output impedance	30	40	50	Ω	High-Ω mode

3.5.1.3 Module-to-Module Interconnect Characteristics

All traces are to be routed as striplines or as microstrips. The tolerance on trace impedance is 10%. Care must be taken when mixing transmission line styles to manage propagation delay differences. The clock delay should be longer than the longest data delay for bus speeds at or above 1.1 Gbps or on lines above 13 cm.

Table 3-11. Processor Interconnect SSB Printed Circuit Board Trace Specifications

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
L_{SSB}	Trace length	—	—	18	cm	For transfer speeds of 1.5 Gbps
				22.5	cm	For transfer speeds of 1.0 Gbps
Z_0	Trace impedance	45	50	55	Ω	
S_{PCB}	Printed circuit board (PCB) data trace skew	—	—	150	ps	

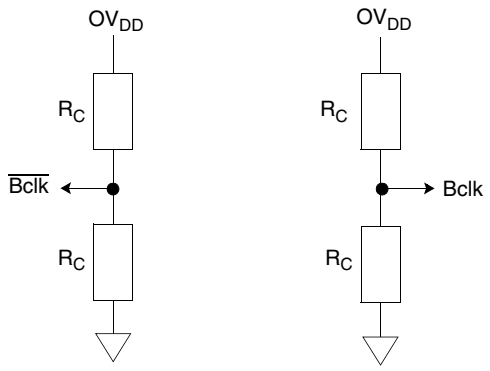
3.5.1.4 Receive Side Characteristics

The receive side contains far-end termination circuitry as shown in *Figure 3-4 Typical Implementation for a Single-Ended Line* on page 31 for the single-ended lines. The total skew from the drive side (S_{DS}) to the module input pins on the receive side (S_{PCB}) is 300 ps (S_{DS} + S_{PCB}) between any two signals (clocks or data). The differential clock termination scheme is shown in *Figure 3-5*. All receivers are pseudo-differential with reference to $V_{REF-SSB}$ and with common-mode rejection of at least 0.5 × V_{DD}. $V_{REF-SSB}$ can be generated internally by the receive-side circuitry or can be derived from the supply voltage.

Table 3-12. Processor Interconnect SSB Receiver Specifications

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
$V_{REF-SSB}$	SSB reference voltage	—	0.5 × OV_{DD}	—	mV	$(V_{OHdc} + V_{OLdc})/2$
$Bclk_{DC}$	Bus clock duty cycle	48	50	52	%	
TR0	Single-ended terminator	83	110	137	Ω	110±25%

Figure 3-5. Differential Clock Termination Circuitry

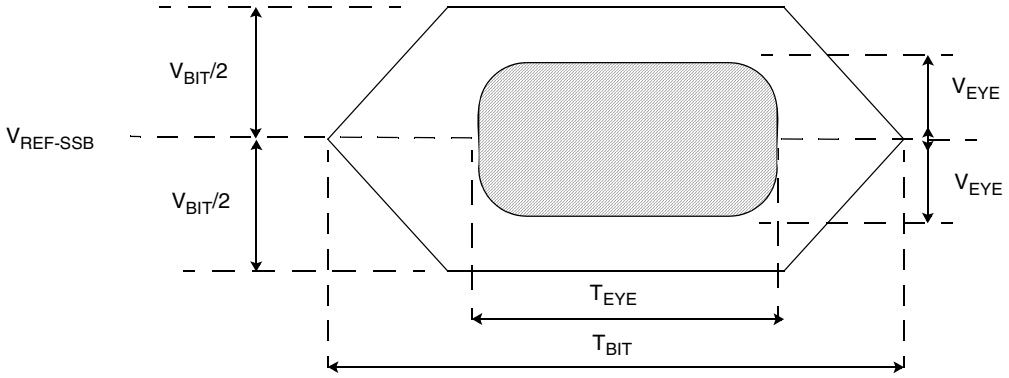


For high-performance operation, the PI supports the inclusion and operation of receive-side circuitry for clock alignment and individual bit-level deskew. An initialization alignment procedure (IAP) is activated at power-on reset (POR) for bit-level deskew and clock alignment. The IAP uses delay elements in the receive-side circuitry to first equalize the delay of the incoming data signals and then center the clock transition in the timing window. The timing parameters for the delay elements and flip-flops that register the data signals are summarized in *Table 3-13*.

Table 3-13. Processor Interconnect SSB Timing Parameters for the Deskew and Clock Alignment

Symbol	Description	Minimum	Typical	Maximum	Units	Notes
T_{BIT}	Bit time		1/(2 × Bclk)		ns	
T_{DED}	Delay element time increment	18	25	35	ps	Thirty-one delay elements for data
T_{DEC}	Delay element time increment	18	25	35	ps	Sixty-four delay elements for clock

Figure 3-6. Post-IAP Eye Opening



The reference level for V_{EYE} is $V_{REF-SSB}$. The horizontal (T_{EYE}) eye opening is a function of the bit time (T_{BIT}) and the earliness of the bus clock transition relative to the slowest data signal.

Table 3-14. Eye-Size Requirements

Bit Rate (Mbps)	Processor to Bus Frequency Ratio	Processor Core (MHz)	Step Time (ps)	Eye Requirement (ps)	Bit Time (ps)	Eye/Bit Time	V_{EYE} (Minimum)
400	3	1200	31.9	863	2500	34.5%	150 mV
450	3	1350	31.9	797	2222.2	34.5%	150 mV
500	3	1500	31.9	744	2000	37.2%	150 mV
500	2	1000	31.9	744	2000	37.2%	150 mV
666	3	1998	27.8	605	1501.5	40.3%	150 mV
666	2	1332	31.9	625	1501.5	41.6%	150 mV
866	2	1732	31.9	544	1154.7	47.1%	150 mV
1066	2	2132	26.0	465	938.1	49.6%	150 mV

3.6 Input ac Specifications

This section provides specifications for the following pins: $\overline{\text{CP0\_INT}}$, $\overline{\text{CP1\_INT}}$, $\overline{\text{MCP}}$, $\overline{\text{CP0\_QACK}}$, $\overline{\text{CP1\_QACK}}$, $\overline{\text{CP0\_HRESET}}$, $\overline{\text{CP1\_HRESET}}$, $\overline{\text{CP0\_SRESET}}$, $\overline{\text{CP1\_SRESET}}$, and TBEN. *Table 3-15*, *Table 3-16* and *Table 3-17* provide the input ac timing specifications as defined in *Figure 3-7 Asynchronous Input Timing* on page 35.

Table 3-15. Input ac Timing Specifications for $\overline{\text{CP0\_INT}}$, $\overline{\text{CP1\_INT}}$, $\overline{\text{MCP}}$, $\overline{\text{CP0\_QACK}}$, $\overline{\text{CP1\_QACK}}$, $\overline{\text{CP0\_SRESET}}$, *and* $\overline{\text{CP1\_SRESET}}$

Callout Number	Characteristic	Value		Unit
		Minimum	Maximum	
1	Rise time	—	< 1	ns
2	Pulse width	10	—	ns
3	Fall time	—	< 1	ns

Table 3-16. Input ac Timing Specifications for $\overline{\text{CP0\_HRESET}}$ *and* $\overline{\text{CP1\_HRESET}}$ [1]

Callout Number	Characteristic	Value		Unit
		Minimum	Maximum	
1	Rise time	—	< 1.5	ns
2	Pulse width	50	—	ns
3	Fall time	—	< 1.5	ns

1. Assumes that the power was previously on and that the PLL is locked. This implies that SYSCLK is running.

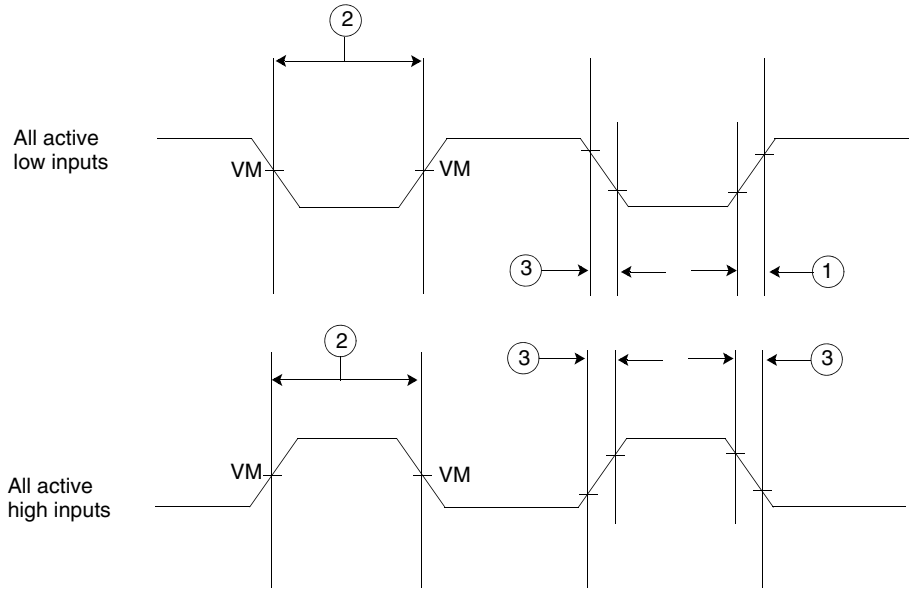
Table 3-17. Input ac Timing Specifications for TBEN

Callout Number	Characteristic	Value		Unit
		Minimum	Maximum	
1	Rise time	—	< 1	ns
2	Pulse width	$8 \times T_{full}$ [1]	—	ns
3	Fall time	—	< 1	ns

1. T_{full} is the clock period of the full-frequency processor clock.

Note: For bus timing information, see *Section 3.5 Processor Interconnect Specifications* on page 30.

Figure 3-7. Asynchronous Input Timing



Notes:

1. No reference to SYSCLK because these inputs are sampled using the internal core clock.
2. Define minimal pulse width as > 1 ns.
3. Define maximum rise and fall times as < 1ns.
4. VM = midpoint voltage ($OV_{DD}/2$).
5. These timings refer to the following pins: $\overline{\text{CP0\_INT}}$, $\overline{\text{CP1\_INT}}$, $\overline{\text{MCP}}$, $\overline{\text{CP0\_QACK}}$, $\overline{\text{CP1\_QACK}}$, $\overline{\text{CP0\_SRESET}}$, $\overline{\text{CP1\_SRESET}}$, $\overline{\text{CP0\_HRESET}}$, $\overline{\text{CP1\_HRESET}}$, and TBEN.
6. The legend for this figure is provided in *Table 3-15* on page 34, *Table 3-16* on page 34 and *Table 3-17* on page 34.
7. Rise and fall times are specified from 20% to 80%.

3.6.1 TBEN Input Pin

The TBEN input pin can be used as either an enable for the internal timebase/decrementer or as an external clock input. The mode is controlled by setting bit 19 of Hardware Implementation Dependent Register 0 (HID0[19]). When this bit is '0', the timebase and decrementer update at 1/16th the processor core frequency whenever TBEN is pulled up to OV_{DD} (traditional enable mode for the internal timebase/decrementer). When HID0[19] is '1', the timebase and decrementer are clocked by the rising edge of TBEN (external clock input mode). When the external clock input mode is used, the TBEN input frequency must not exceed 1/16th of the core processor maximum frequency.

3.7 Asynchronous Output Specifications

This section describes the asynchronous output and bidirectional (BiDi) signals. Timing information is not provided because these signals are launched by the internal core clock.

Table 3-18, *Table 3-19*, and *Table 3-20* list the asynchronous output and bidirectional signals.

Table 3-18. Asynchronous Type Output Signals

Pin	Description	Comment	Pin
ATTENTION	Attention	To service processor	AC7
$\overline{\text{CP0\_QREQ}}$	Quiesce request	Power management - core 0	AB9
$\overline{\text{CP1\_QREQ}}$	Quiesce request	Power management - core 1	AC21
TRIGGEROUT		Debug only	R22

Note: There is no reference to SYSCLK because this output is launched by the (internal) core clock.

Table 3-19. Asynchronous Open-Drain Output Signals

Pin	Description	Comment	Pin
I2CGO	I^2C interface go	Arbitration I^2C and JTAG	E13

Notes:
- The rise and fall times are measured between the 20% to 80% of the input signal swing voltages.
- There is no reference to SYSCLK because this output is launched by the (internal) core clock.
- Pull-up resistor = 4.7 kΩ. (Any value > 200 Ω should ensure a good down level, but it depends on the signal loading.)

Table 3-20. Asynchronous Open-Drain Bidirectional Signals

Pin	Description	Comment	Pin
$\overline{\text{CHKSTOP}}$	Checkstop signal input/output		T22

Notes:
- There is no reference to SYSCLK because this output is launched by the (internal) core clock.
- Pull-up resistor = 5 kΩ. (Any value > 200 Ω should ensure a good down level, but it depends on the signal loading.)

3.8 Mode Select Input Timing Specifications

This section provides timing specifications for the mode-select pins. These pins are sampled by $\overline{\text{CP0\_HRESET}}$.

Table 3-21 provides the input ac timing specifications as defined in *Figure 3-8* on page 38. The mode-select signals and debug pins are listed in *Table 3-22* on page 38 and *Table 3-23* on page 39.

Table 3-21. Input ac Timing Specifications

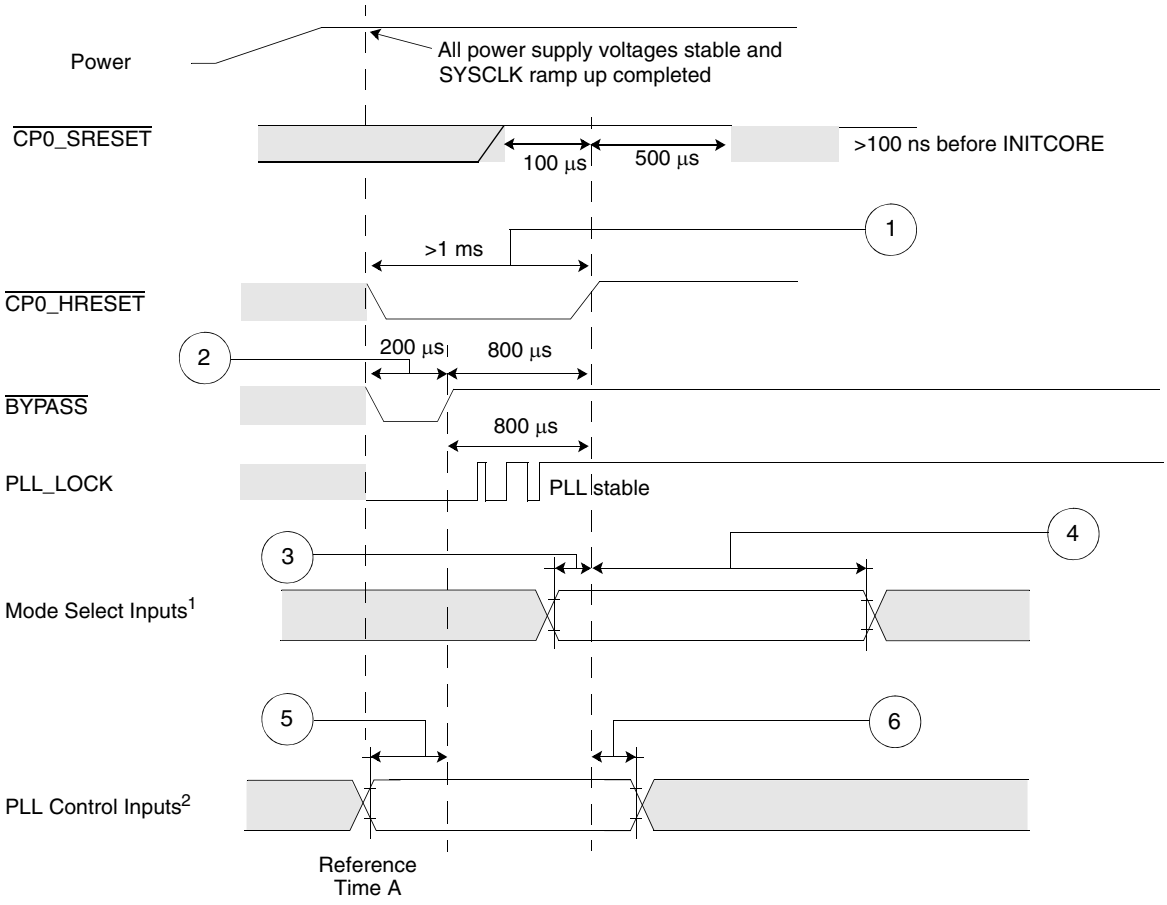
Callout Number	Characteristic	Value		Unit	Notes
		Minimum	Maximum		
1	$\overline{\text{CP0\_HRESET}}$ width	> 1	—	ms	1
2	$\overline{\text{BYPASS}}$ width	200	—	µs	—
3	Mode select signals	20	—	Core clocks	2, 3
4	Mode select inputs hold time	1000	—	Core clocks	2
5	PLL control signals	20	—	Core clocks	4, 5
6	PLL control inputs hold time	20	—	Core clocks	4, 5

Notes:

1. $\overline{\text{CP0\_HRESET}}$ pulse width covers resetting the PLL ($\overline{\text{BYPASS}}$ Width) + 800 microseconds required for the PLL to lock. The POR sequence can only start if the PLL is locked.
2. Mode select pins must not change level sooner than 20 core clocks before the rising edge of $\overline{\text{CP0\_HRESET}}$ and must be held for a minimum of 1000 core clocks after the rising edge of $\overline{\text{CP0\_HRESET}}$.
3. Guaranteed by design and not tested.
4. PLL control pins must not change level earlier than 20 core clocks before the rising edge of $\overline{\text{BYPASS}}$ and must be held for a minimum of 20 core clocks after the rising edge of $\overline{\text{CP0\_HRESET}}$.
5. PLL control inputs must not change while $\overline{\text{CP0\_HRESET}}$ is low.

Note: For bus timing information, see *Section 3.5 Processor Interconnect Specifications* on page 30.

Figure 3-8. CP0_HRESET and BYPASS Timing Diagram



Notes:

1. These timings refer to the following pins: BUS_CFG(0:2) and PROCID(0:1).
2. These timings refer to the following pins: CKTERM_DIS, PLL_MULT, and PLL_RANGE(1:0). These pins can only be changed by driving CP0_HRESET and BYPASS low.
3. CP0_HRESET and BYPASS might be low during initial program load (IPL) stages and not have to transition power before reference time A.
4. PLL control inputs must not change while CP0_HRESET is low.
5. The legend for this figure is provided in *Table 3-21* on page 37.

Table 3-22. Mode Select Type Input Signals

Pin Name	Description	Comment	Pin Location
BUS_CFG(0:2)	Bus configuration	Select core clock to bus clock ratio.	A11, D12, B11
CKTERM_DIS	Clock receiver termination	Disables the 50 Ω parallel SYSCLK termination. Pulled up to OV_{DD} for applications using external termination on SYSCLK and SYSCLK. Otherwise, pulled low to GND.	Y5
PLL_MULT	Select between multiplier 8 or 12		AC5
PLL_RANGE(1:0)	PLL range select		AD3, AA4
PROCID(0:1)	Processor identifier (ID)	For use in a multiprocessor environment.	N21, N22

Table 3-23. Debug Pins

Pin Name	Description	Comment	Pin Location
$\overline{\text{AVP\_RESET}}$	Changes the POR sequence.	For manufacturing test only.	U24
EI_DISABLE	Disables the initial alignment procedure (IAP)	Disables the use of IAP to adjust clock skew on the processor interface.	B12
GPULDBG	PowerPC 970MP POR in debug mode	See the *PowerPC 970MP Power-On Reset Application Note* for additional details. 10 KΩ pull up to OV_{DD}.	Y24

3.9 Spread Spectrum Clock Generator

3.9.1 Design Considerations

When designing with the spread spectrum clock generator (SSCG), there are a several design issues that must be considered as described in this section. SSCG creates a controlled amount of long-term jitter. For a receiving PLL in the PowerPC 970MP to operate in this environment, it must be able to accurately track the SSCG clock jitter.

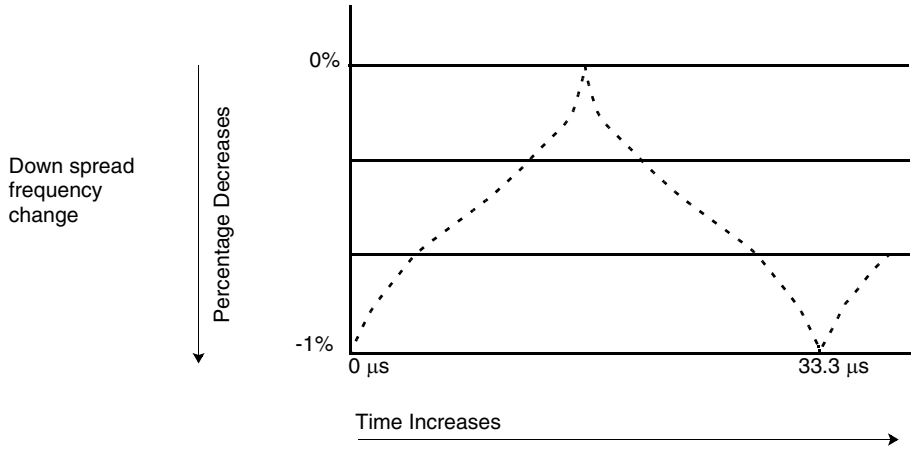
Note: The accuracy to which the PowerPC 970MP PLL can track the SSCG clock is called the *tracking skew*.

The following SSCG configuration is recommended:

- Down spread mode less than or equal to 1% of the maximum frequency
- A modulation frequency of 30 kHz
- A cubic sweep profile, also called a Hershey's Kiss profile (as in a Lexmark[1] profile), as shown in *Figure 3-9*

In this configuration the tracking skew is less than 100 ps.

Figure 3-9. SSCG *Modulation Profile*



1. See patent 5,631,920.

3.10 I²C and JTAG

The single external I²C interface connects to two I²C controllers, one for each processing unit. The controllers are distinguished by the low-order address bit, which is '0' for processing unit 0 and '1' for processing unit 1. Similarly, the single external JTAG interface connects to two daisy-chained JTAG controllers, one for each processing unit.

3.10.1 I²C Bus Timing Information

The I²C bus specification can be downloaded from NXP Web site at http://www.nxp.com/products/interface_control/i2c/.

The PowerPC 970MP I²C bus conforms to the standard-mode timing specification and does not support the high-speed (Hs-mode) or fast-mode timing. The default I²C bus speed for the PowerPC 970MP is 50 kHz. A scan communication (SCOM) write with the I²C bus running at 50 kHz is needed to allow the bus to conform to the standard-mode timing specification of 100 kHz. See the *PowerPC 970MP Power-On Reset Application Note* for more details.

The PowerPC 970MP I²C pins are limited to OV_{DD} voltages. Level shifting or pullups or both might be required to interface to higher voltage devices. See *The I²C bus specification* for recommendations on level shifting and pullups.

Notes:

1. To avoid problems, level shifted PPC970MP I²C bus pins must not be wired together with non-PowerPC 970MP parts in a system. The PowerPC 970MP should have its own private level shifter.
2. If one level shifter is used for multiple PowerPC 970MP microprocessors, the length of the traces must be controlled very carefully.

3.10.2 JTAG ac Timing Specifications

Table 3-24 JTAG ac Timing Specifications (Dependent on SYSCLK) on page 42 provides the JTAG (IEEE 1149.1) ac timing specifications as defined in *Figure 3-10 JTAG Clock Input Timing Diagram* on page 42 and *Figure 3-11 Test Access Port Timing Diagram* on page 43. The five JTAG signals are as follows:

1. TDI (test data in)
2. TDO (test data out)
3. TMS (test mode select)
4. TCK (test clock)
5. $\overline{\text{TRST}}$ (test reset)

Note: The PowerPC 970MP diverges from the standard IEEE ac timing implementation in this regard:

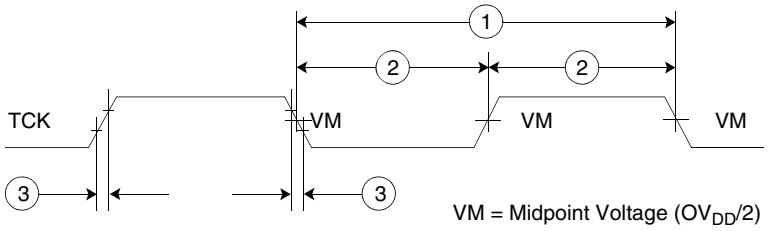
JTAG is normally used with the PLL running; however, it can also be used with the PLL in bypass mode. If the PLL is in bypass mode, clock pulses must be supplied to the SYSCLK and $\overline{\text{SYSCLK}}$ pins at a rate 40 times higher than the TCK rate.

Table 3-24. JTAG ac Timing Specifications (Dependent on SYSCLK)

Callout Number	Characteristic	Minimum	Maximum	Unit	Notes
—	TCK frequency of operation	—	1/40	Core processor frequency	1, 5
1	TCK cycle time	40	—	Core clocks	2, 5
2	TCK clock pulse width	20	—	Core clocks	2, 5
3	TCK rise and fall times	0	2	ns	3, 5
4	TMS, TDI data setup time	0	—	ns	5
5	TMS, TDI data hold time	15	—	ns	5
6	TCK to TDO data valid	2.5	12	ns	4, 5
7	TCK to TDO high impedance	3	9	ns	3, 5
8	TCK to output data invalid (output hold)	0	—	ns	5

Notes:
1. TCK frequency is limited by the core processor frequency.
2. Core clock cycles.
3. Guaranteed by characterization and not tested.
4. Minimum specification guaranteed by characterization and not tested.
5. JTAG timings are dependent on an active SYSCLK.
6. For timing diagrams, see *Figure 3-10 JTAG Clock Input Timing Diagram* and *Figure 3-11 Test Access Port Timing Diagram* on page 43.

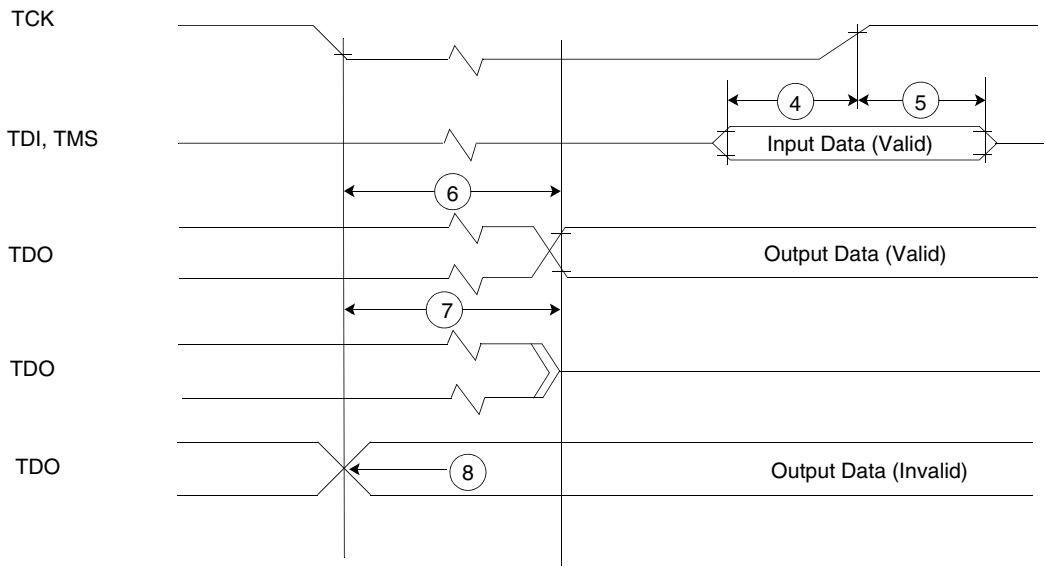
Figure 3-10. JTAG Clock Input Timing Diagram



Note: The legend for this figure is provided in *Table 3-24*.

Figure 3-11 provides the test access port timing diagram.

Figure 3-11. Test Access Port Timing Diagram



Note: The legend for this figure is provided in *Table 3-24 JTAG ac Timing Specifications (Dependent on SYSCLK)* on page 42.

3.10.3 I^{2}C and JTAG Considerations

The PowerPC 970MP supports I^{2}C and JTAG. The I^{2}C data and clock pins as well as the TCK, TMS, TDI, and $\overline{\text{TRST}}$ pins should be pulled up to OV_{DD}. Use of the I^{2}C or JTAG bus is mutually exclusive and controlled by the I2CSEL pin. If this pin is high, the I^{2}C bus can be used. If the pin is low, the JTAG bus can be used. Traffic on the nonselected bus (I^{2}C or JTAG depending on I2CSEL) is ignored and does not have any side effect.

3.10.3.1 Guidance for Using Both I^{2}C and JTAG

If selective use of both interfaces is required, then the I2CSEL pin can be switched while the system is running. For correct operation, it is recommended to switch the I2CSEL pin only while no traffic is active on either interface to prevent misrecognition of a partial transmission. To ease this operation in debug mode (GPULDBG = '1'), the I2CGO pin can be monitored or directly connected to the I2CSEL pin. This pin will switch from '0' to '1' whenever it is safe to switch I2CSEL from '0' to '1' for I^{2}C usage. Similarly, it will switch from '1' to '0' whenever it is safe to switch I2CSEL from '1' to '0' for JTAG usage. See the *PowerPC 970MP Power-On Reset Application Note* for a description of how the I2CGO pin is controlled by software.

3.10.4 Boundary Scan Considerations

The PowerPC 970MP does not support the boundary scan description language (BSDL) standard for implementing boundary scan testing. Boundary scan patterns are available for customer use, but require other signals to be controlled in addition to the JTAG port. Boundary scan testing requires an input clock (SYSCLK and $\overline{\text{SYSCLK}}$) and control of $\overline{\text{CP0\_HRESET}}$.

4. Dimensions and Physical Signal Assignments

The PowerPC 970MP uses a ceramic ball grid array (CBGA) that supports 575 balls. The PowerPC 970MP is offered in a reduced-lead package with SnAgCu (SAC) balls.

Note: All lead free or reduced-lead ball grid array (BGA) modules are classified as JEDEC Moisture Sensitive Level 3.

The following sections contain several views of the package, pin information, and a pin listing.

4.1 Electrostatic Discharge Considerations

This product has been electrostatic discharge (ESD) tested to meet or exceed the Joint Electron Device Engineering Council (JEDEC) specifications for the following models:

- Human body model (HBM) - Class 1B
- Field-induced charged device model (CDM) - Class II
- Machine model (MM) - Class A

Note: Appropriate ESD handling procedures should be implemented and maintained for any facilities handling this component.

4.2 Mechanical Packaging

Figure 4-1 PowerPC 970MP Mechanical Package (Side and Top View) on page 47 shows the side and top views of the packages including the height from the top of the die to the bottom of the solder balls. *Figure 4-2 PowerPC 970MP Mechanical Package (Bottom View)* on page 48 shows a bottom view of the PowerPC 970MP.

4.2.1 Reduced-Lead Package

This is a reduced-lead package as indicated by the ‘R’ in the package code field of the part number. It uses lead-free solder for the substrate capacitors and the BGA balls on the bottom of the package. Standard high-melting-point 97% Pb and 3% Sn solder (exempted by the European Union restriction of hazardous substances [RoHS] legislation) is used for the C4 balls that connect the die to the substrate. The resulting module is RoHS compatible.

4.2.1.1 Mechanical Specifications

Table 4-1. Package Layout and Assembly Specifications

Package	JEDEC Moisture Sensitivity Level (MSL)	Solder Ball Composition	Solder Ball Diameter mm (inch)	CBGA Substrate I/O Pad Diameter mm (inch)	Card Solder Mask Opening Diameter mm (inch)	Card Solder Screen Diameter	Card Pad Diameter mm (inch)
Reduced Lead	3	Sn 95.5% Ag 3.8% Cu 0.7%	0.635 (25)	0.80 (31.5)	0.72 (28)	23 mil opening in 4 mil thick stencil, 1400-2000 cubic mils	0.61 (24)

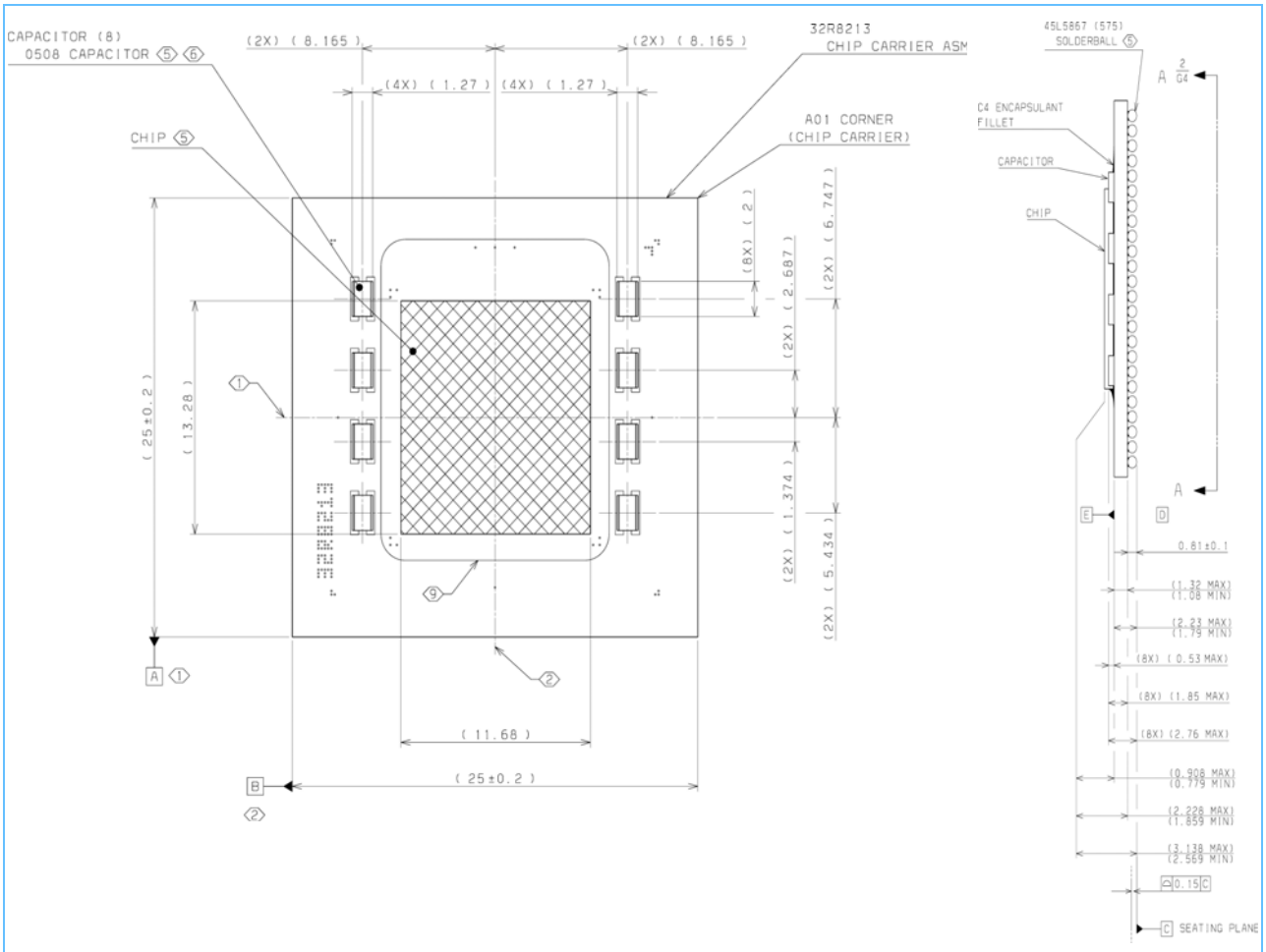
Note: All dimensions are in mm unless otherwise noted. Dimensions in parenthesis are in inches.

4.2.1.2 Assembly Considerations

This reduced-lead package is compatible with a 260°C lead-free card assembly reflow profile. See the International Electronics Manufacturing Initiative (iNEMI) Consortium, www.inemi.org, for industry-standard assembly and rework information. The coplanarity specification for the reduced-lead CBGA, like other single-melt BGA packages, is 0.20 mm (8 mils). The qualification testing included a lead-free, water-soluble solder paste with type 3 mesh size (-325±500). The solder alloy is 95.5% Sn, 4.0% Ag, and 0.5% Cu, with a 90% metal loading. The paste viscosity range is 600 to 800 thousands of centipoises (kcps). The thickness of the stencil is 4 mils, and the aperture diameter is 23 mils. The target solder paste volume range is between 1400 to 2000 cubic mils. Achieving the correct paste volume is necessary to eliminate solder shorts and produce high reliability solder joints. The actual solder paste volume from the qualification build ranged from 1750 to 2000 cubic mils.

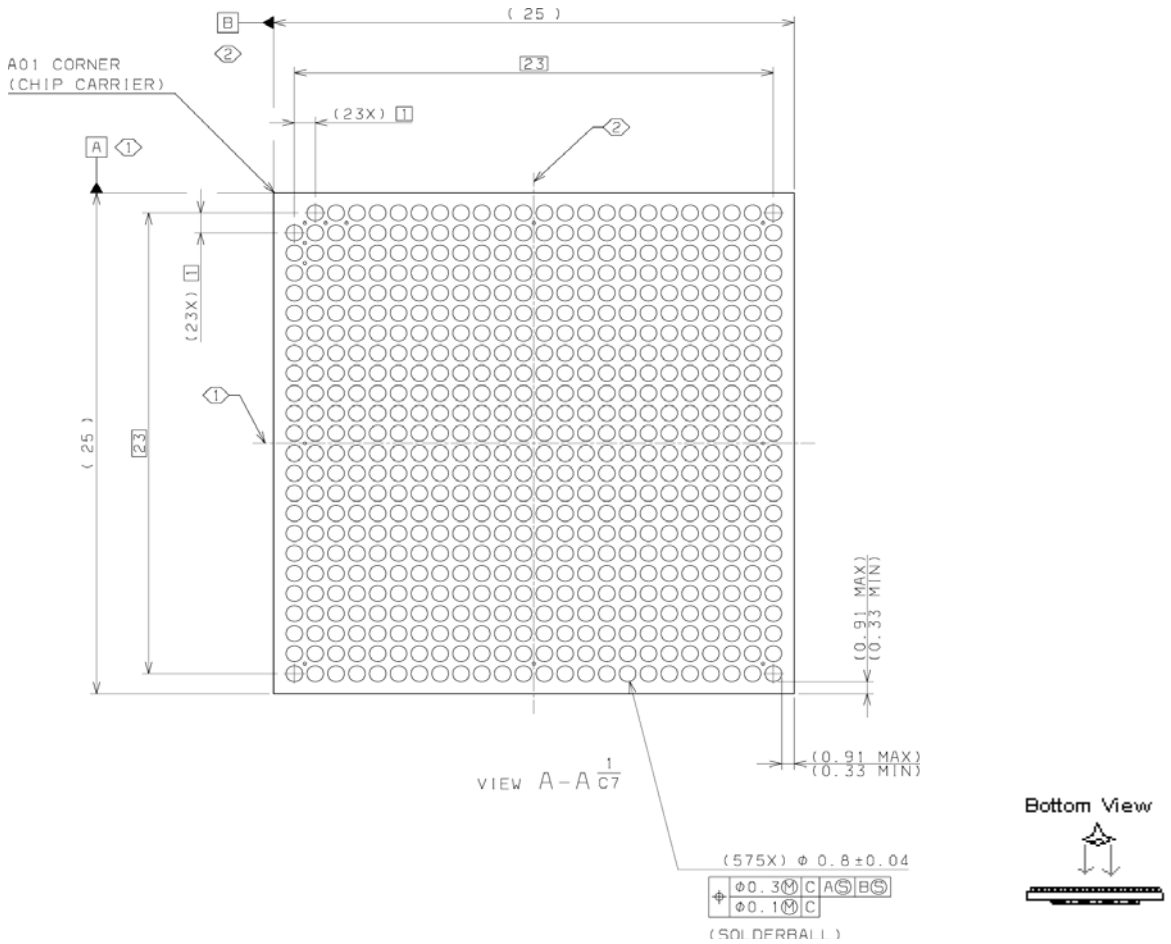
As shown in *Table 4-1*, the JEDEC moisture sensitivity level is MSL 3. Storage and assembly protocols should be modified accordingly.

Figure 4-1. PowerPC 970MP Mechanical Package (Side and Top View) (Preliminary)



Legend	
1	DATUM A is the center plane of the feature labeled DATUM A.
2	DATUM B is the center plane of the feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about the center lines defined by DATUMs A and B.
4	Where not otherwise defined, the center lines indicated are to be interpreted as a datum framework, established by DATUM D, A, and B respectively.
9	This line defines the approximate boundary configuration of encapsulant as dispensed.
10	The chip's assembled height (which includes silicon thickness and melted C4) for 300 mm wafers is: 0.829 - 0.908 mm. The 300 mm silicon thickness is 0.785 ±0.020 mm.

Figure 4-2. PowerPC 970MP Mechanical Package (Bottom View) (Preliminary)



Legend	
1	DATUM A is the center plane of the feature labeled DATUM A.
2	DATUM B is the center plane of the feature labeled DATUM B.
3	Unless otherwise specified, the part is symmetrical about the center lines defined by DATUMs A and B.
4	Where not otherwise defined, the center lines indicated are to be interpreted as a datum framework, established by DATUM D, A, and B respectively.
9	This line defines the approximate boundary configuration of encapsulant as dispensed.
10	The chip's assembled height (which includes silicon thickness and melted C4) for 300 mm wafers is: 0.829 - 0.908 mm. The 300 mm silicon thickness is 0.785±0.020 mm.

Table 4-2. PowerPC 970MP Ball Placement (Top View)

AD24 BI_MODE	AD23 GND	AD22 TMS	AD21 CP0_OA CK	AD20 CP1_IN T	AD19 GND	AD18 CP1_QA CK	AD17 CP1_FRED_EN	AD16 GND	AD15 TBEN	AD14 GND	AD13 V1	AD12 GND	AD11 V0	AD10 PULSE_SEL2	AD9 V0	AD8 TDO	AD7 V0	AD6 SPARE1	AD5 GND	AD4 OV_{DD}	AD3 PLL_RANGE1	AD2 GND	AD1 OV_{DD}	AD
AC24 CP1_DIODE_NEG	AC23 OV_{DD}	AC22 GND	AC21 CP1_QR EQ	AC20 OV_{DD}	AC19 V1	AC18 GND	AC17 OV_{DD}	AC16 CP1_HR ESET	AC15 V1	AC14 LSSD_STOP_ENABLE	AC13 OV_{DD}	AC12 CP0_FRED_GND	AC11 GND	AC10 GND	AC9 OV_{DD}	AC8 GND	AC7 ATTENTION	AC6 V0	AC5 PLL_MULT	AC4 V0	AC3 SPARE2	AC2 OV_{DD}	AC1 GND	AC
AB24 CP1_DIODE_POS	AB23 TCK	AB22 CP1_SR ESET	AB21 V1	AB20 V1	AB19 GND	AB18 V1	AB17 C1_UND_GLOBAL	AB16 V1	AB15 C2_UND_GLOBAL	AB14 V1	AB13 CP0_IN T	AB12 V1	AB11 LSSD_STOPC2_ENABLE	AB10 V0	AB9 CP0_QR EQ	AB8 OV_{DD}	AB7 CP0_SR ESET	AB6 V0	AB5 GND	AB4 CP0_KELV_V0	AB3 V0	AB2 GND	AB1 OV_{DD}	AB
AA24 GND	AA23 TDI	AA22 V1	AA21 MCP	AA20 GND	AA19 V1	AA18 GND	AA17 V1	AA16 GND	AA15 V1	AA14 GND	AA13 TRST	AA12 GND	AA11 V0	AA10 GND	AA9 CP0_HR ESET	AA8 GND	AA7 V0	AA6 GND	AA5 V0	AA4 PLL_RANGE0	AA3 V0	AA2 GND	AA1 GND	AA
Y24 GPULDBG	Y23 V1	Y22 GND	Y21 PSRO_ENABLE	Y20 V1	Y19 GND	Y18 V1	Y17 GND	Y16 V1	Y15 GND	Y14 V1	Y13 GND	Y12 CP1_FRED_GND	Y11 CP0_FRED_EN	Y10 OV_{DD}	Y9 GND	Y8 V0	Y7 GND	Y6 V0	Y5 CKTERM_DIS	Y4 CP0_DIODE_NEG	Y3 CP0_DIODE_POS	Y2 V0	Y1 OV_{DD}	Y
W24 SYNC_ENABLE	W23 OV_{DD}	W22 CP1_KELV_GND1	W21 CP1_KELV_V1	W20 GND	W19 V1	W18 GND	W17 V1	W16 GND	W15 V1	W14 OV_{DD}	W13 V0	W12 GND	W11 OV_{DD}	W10 GND	W9 V0	W8 GND	W7 V0	W6 GND	W5 V0	W4 RI	W3 GND	W2 CP0_KELV_GND0	W1 GND	W
V24 I2CCK	V23 GND	V22 I2CDT	V21 GND	V20 V1	V19 GND	V18 V1	V17 GND	V16 V1	V15 GND	V14 V1	V13 GND	V12 V0	V11 GND	V10 V0	V9 GND	V8 V0	V7 GND	V6 V0	V5 GND	V4 V0	V3 CP0_PSRO0	V2 V0	V1 PULSE_SEL0	V
U24 AVP_RESET	U23 PLLLOCK	U22 LSSD_SCAN_ENABLE	U21 V1	U20 GND	U19 V1	U18 GND	U17 V1	U16 GND	U15 V1	U14 GND	U13 V1	U12 GND	U11 V0	U10 GND	U9 V0	U8 GND	U7 V0	U6 GND	U5 V0	U4 GND	U3 LSSD_STOP_C2STAR_ENABLE	U2 LSSDMODE	U1 I2CSEL	U
T24 BYPASS	T23 OV_{DD}	T22 CHKSTOP	T21 GND	T20 V1	T19 GND	T18 V1	T17 GND	T16 V1	T15 GND	T14 V1	T13 GND	T12 V0	T11 GND	T10 V0	T9 GND	T8 V0	T7 GND	T6 V0	T5 GND	T4 V0	T3 PULSE_SEL1	T2 LSSD_RAMSTOP_ENABLE	T1 V0	T
R24 DI2	R23 GND	R22 TRIGGEROUT	R21 V1	R20 GND	R19 V1	R18 GND	R17 V1	R16 GND	R15 V1	R14 GND	R13 V1	R12 GND	R11 V0	R10 GND	R9 V0	R8 GND	R7 V0	R6 GND	R5 V0	R4 GND	R3 V0	R2 MASTERSEL	R1 GND	R
P24 GND	P23 GND	P22 V1	P21 GND	P20 V1	P19 GND	P18 V1	P17 GND	P16 V1	P15 GND	P14 V1	P13 GND	P12 V0	P11 GND	P10 V0	P9 GND	P8 V0	P7 GND	P6 V0	P5 GND	P4 PSYNC	P3 Z_OUT	P2 GND	P1 Z_SENSE	P
N24 SRIN0	N23 V1	N22 PROCID1	N21 PROCID0	N20 GND	N19 V1	N18 GND	N17 V1	N16 GND	N15 V1	N14 GND	N13 V1	N12 GND	N11 V0	N10 GND	N9 V0	N8 GND	N7 V0	N6 GND	N5 V0	N4 GND	N3 GND	N2 ADOUT0	N1 OV_{DD}	N
M24 SRIN0	M23 OV_{DD}	M22 V1	M21 GND	M20 V1	M19 GND	M18 V1	M17 GND	M16 V1	M15 GND	M14 V1	M13 GND	M12 V0	M11 GND	M10 V0	M9 GND	M8 V0	M7 GND	M6 V0	M5 GND	M4 V0	M3 OV_{DD}	M2 ADOUT4	M1 SROUT0	M
L24 ADIN8	L23 SRIN1	L22 GND	L21 V1	L20 V1	L19 V1	L18 GND	L17 V1	L16 GND	L15 V1	L14 GND	L13 V1	L12 GND	L11 V0	L10 GND	L9 V0	L8 GND	L7 V0	L6 GND	L5 V0	L4 OV_{DD}	L3 GND	L2 ADOUT3	L1 SROUT0	L
K24 GND	K23 SRIN1	K22 ADIN6	K21 GND	K20 OV_{DD}	K19 GND	K18 V1	K17 GND	K16 V1	K15 GND	K14 V1	K13 GND	K12 V0	K11 GND	K10 V0	K9 GND	K8 V0	K7 GND	K6 V0	K5 OV_{DD}	K4 GND	K3 ADOUT5	K2 ADOUT6	K1 GND	K
J24 ADIN2	J23 ADIN7	J22 GND	J21 OV_{DD}	J20 GND	J19 V1	J18 GND	J17 V1	J16 GND	J15 V1	J14 GND	J13 V0	J12 GND	J11 V0	J10 GND	J9 V0	J8 GND	J7 V0	J6 GND	J5 V0	J4 GND	J3 OV_{DD}	J2 ADOUT2	J1 ADOUT8	J
H24 OV_{DD}	H23 ADIN0	H22 ADIN3	H21 GND	H20 V0	H19 GND	H18 V1	H17 GND	H16 V1	H15 GND	H14 V1	H13 GND	H12 V0	H11 GND	H10 V0	H9 GND	H8 V0	H7 GND	H6 V0	H5 OV_{DD}	H4 GND	H3 ADOUT7	H2 GND	H1 SROUT1	H
G24 ADIN13	G23 ADIN1	G22 V1	G21 V0	G20 OV_{DD}	G19 V1	G18 GND	G17 V1	G16 GND	G15 V1	G14 OV_{DD}	G13 V0	G12 GND	G11 V0	G10 GND	G9 V0	G8 GND	G7 V0	G6 GND	G5 GND	G4 GND	G3 ADOUT1	G2 GND	G1 SROUT1	G
F24 GND	F23 ADIN14	F22 OV_{DD}	F21 GND	F20 GND	F19 OV_{DD}	F18 V0	F17 V1	F16 OV_{DD}	F15 GND	F14 V0	F13 GND	F12 SYSCLK	F11 GND	F10 V0	F9 OV_{DD}	F8 V0	F7 GND	F6 OV_{DD}	F5 V0	F4 OV_{DD}	F3 ADOUT13	F2 OV_{DD}	F1 ADOUT10	F
E24 ADIN11	E23 GND	E22 ADIN9	E21 ADIN21	E20 ADIN31	E19 ADIN32	E18 GND	E17 ADIN30	E16 ADIN29	E15 ADIN18	E14 OV_{DD}	E13 I2CGO	E12 SYSCLK	E11 OV_{DD}	E10 ADOUT15	E9 ADOUT18	E8 ADOUT39	E7 ADOUT23	E6 OV_{DD}	E5 ADOUT21	E4 ADOUT32	E3 ADOUT9	E2 GND	E1 ADOUT12	E
D24 OV_{DD}	D23 ADIN10	D22 OV_{DD}	D21 ADIN23	D20 GND	D19 OV_{DD}	D18 ADIN27	D17 ADIN35	D16 OV_{DD}	D15 ADIN15	D14 GND	D13 PLLTEST	D12 BUS_CFG1	D11 GND	D10 ADOUT16	D9 ADOUT41	D8 OV_{DD}	D7 ADOUT35	D6 ADOUT36	D5 GND	D4 ADOUT31	D3 ADOUT11	D2 CLKOUT	D1 CLKOUT	D
C24 CLKIN	C23 GND	C22 ADIN22	C21 ADIN20	C20 ADIN33	C19 ADIN34	C18 ADIN43	C17 ADIN42	C16 ADIN19	C15 ADIN40	C14 ADIN28	C13 OV_{DD}	C12 PLLTESTOUT	C11 OV_{DD}	C10 ADOUT28	C9 ADOUT40	C8 GND	C7 ADOUT14	C6 ADOUT27	C5 ADOUT33	C4 OV_{DD}	C3 ADOUT25	C2 OV_{DD}	C1 ADOUT26	C
B24 CLKIN	B23 ADIN25	B22 ADIN24	B21 OV_{DD}	B20 ADIN36	B19 OV_{DD}	B18 ADIN39	B17 GND	B16 OV_{DD}	B15 ADIN16	B14 ADIN4	B13 KELV_GND2	B12 EI_DISABLE	B11 BUS_CFG2	B10 GND	B9 ADOUT17	B8 ADOUT19	B7 OV_{DD}	B6 ADOUT43	B5 ADOUT30	B4 ADOUT37	B3 GND	B2 ADOUT20	B1 GND	B
A24 OV_{DD}	A23 ADIN12	A22 GND	A21 ADIN37	A20 GND	A19 ADIN38	A18 ADIN26	A17 ADIN41	A16 ADIN17	A15 ADIN5	A14 GND	A13 ANALOGGND	A12 AVDD	A11 BUS_CFG0	A10 KELV_OVDD	A9 ADOUT29	A8 ADOUT38	A7 ADOUT42	A6 ADOUT34	A5 GND	A4 ADOUT24	A3 OV_{DD}	A2 ADOUT22		A
24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 4-3. PowerPC 970MP Ball Placement (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
AD	AD1 OVDD	AD2 GND	AD3 PLL_RANGE1	AD4 OVDD	AD5 GND	AD6 SPARE1	AD7 V0	AD8 TDO	AD9 V0	AD10 PULSE_SEL2	AD11 V0	AD12 GND	AD13 V1	AD14 GND	AD15 TBEN	AD16 GND	AD17 CP1_FRED_EN	AD18 CP1_OACK	AD19 GND	AD20 CP1_INT	AD21 CP0_OACK	AD22 TMS	AD23 GND	AD24 BI_MODE
AC	AC1 GND	AC2 OVDD	AC3 SPARE2	AC4 V0	AC5 PLL_MULT	AC6 V0	AC7 ATTENTION	AC8 GND	AC9 OVDD	AC10 GND	AC11 GND	AC12 CP0_FRED_GND	AC13 OVDD	AC14 LSSD_STOP_ENABLE	AC15 V1	AC16 CP1_HRESET	AC17 OVDD	AC18 GND	AC19 V1	AC20 OVDD	AC21 CP1_QREQ	AC22 GND	AC23 OVDD	AC24 CP1_DIODE_NEG
AB	AB1 OVDD	AB2 GND	AB3 V0	AB4 CP0_KELV_V0	AB5 GND	AB6 V0	AB7 CP0_SRESET	AB8 OVDD	AB9 CP0_QREQ	AB10 V0	AB11 LSSD_STOPC2_ENABLE	AB12 V1	AB13 CP0_INT	AB14 V1	AB15 C2_UND_GLOBAL	AB16 V1	AB17 C1_UND_GLOBAL	AB18 V1	AB19 GND	AB20 V1	AB21 V1	AB22 CP1_SRESET	AB23 TCK	AB24 CP1_DIODE_POS
AA	AA1 GND	AA2 GND	AA3 V0	AA4 PLL_RANGE0	AA5 V0	AA6 GND	AA7 V0	AA8 GND	AA9 CP0_HRESET	AA10 GND	AA11 V0	AA12 GND	AA13 TRST	AA14 GND	AA15 V1	AA16 GND	AA17 V1	AA18 GND	AA19 V1	AA20 GND	AA21 MCP	AA22 V1	AA23 TDI	AA24 GND
Y	Y1 OVDD	Y2 V0	Y3 CP0_DIODE_POS	Y4 CP0_DIODE_NEG	Y5 CKTERM_DIS	Y6 V0	Y7 GND	Y8 V0	Y9 GND	Y10 OVDD	Y11 CP0_FRED_EN	Y12 CP1_FRED_GND	Y13 GND	Y14 V1	Y15 GND	Y16 V1	Y17 GND	Y18 V1	Y19 GND	Y20 V1	Y21 PSRO_ENABLE	Y22 GND	Y23 V1	Y24 GPULDBG
W	W1 GND	W2 CP0_KELV_GND0	W3 GND	W4 RI	W5 V0	W6 GND	W7 V0	W8 GND	W9 V0	W10 GND	W11 OVDD	W12 GND	W13 V0	W14 OVDD	W15 V1	W16 GND	W17 V1	W18 GND	W19 V1	W20 GND	W21 CP1_KELV_V1	W22 CP1_KELV_GND1	W23 OVDD	W24 SYNC_ENABLE
V	V1 PULSE_SEL0	V2 V0	V3 CP0_PSRO0	V4 V0	V5 GND	V6 V0	V7 GND	V8 V0	V9 GND	V10 V0	V11 GND	V12 V0	V13 GND	V14 V1	V15 GND	V16 V1	V17 GND	V18 V1	V19 GND	V20 V1	V21 GND	V22 I2CDT	V23 GND	V24 I2CCK
U	U1 I2CSEL	U2 LSSDMODE	U3 LSSD_STOP_C2STAR_ENABLE	U4 GND	U5 V0	U6 GND	U7 V0	U8 GND	U9 V0	U10 GND	U11 V0	U12 GND	U13 V1	U14 GND	U15 V1	U16 GND	U17 V1	U18 GND	U19 V1	U20 GND	U21 V1	U22 LSSD_SCAN_ENABLE	U23 PLLLOCK	U24 AVP_RESET
T	T1 V0	T2 LSSD_RAMSTOP_ENABLE	T3 PULSE_SEL1	T4 V0	T5 GND	T6 V0	T7 GND	T8 V0	T9 GND	T10 V0	T11 GND	T12 V0	T13 GND	T14 V1	T15 GND	T16 V1	T17 GND	T18 V1	T19 GND	T20 V1	T21 GND	T22 CHKSTOP	T23 OVDD	T24 BYPASS
R	R1 GND	R2 MASTERSEL	R3 V0	R4 GND	R5 V0	R6 GND	R7 V0	R8 GND	R9 V0	R10 GND	R11 V0	R12 GND	R13 V1	R14 GND	R15 V1	R16 GND	R17 V1	R18 GND	R19 V1	R20 GND	R21 V1	R22 TRIGGEROUT	R23 GND	R24 DI2
P	P1 Z_SENSE	P2 GND	P3 Z_OUT	P4 PSYNC	P5 GND	P6 V0	P7 GND	P8 V0	P9 GND	P10 V0	P11 GND	P12 V0	P13 GND	P14 V1	P15 GND	P16 V1	P17 GND	P18 V1	P19 GND	P20 V1	P21 GND	P22 V1	P23 GND	P24 GND
N	N1 OVDD	N2 ADOUT0	N3 GND	N4 GND	N5 V0	N6 GND	N7 V0	N8 GND	N9 V0	N10 GND	N11 V0	N12 GND	N13 V1	N14 GND	N15 V1	N16 GND	N17 V1	N18 GND	N19 V1	N20 GND	N21 PROCID0	N22 PROCID1	N23 V1	N24 SRIN0
M	M1 SROUT0	M2 ADOUT4	M3 OVDD	M4 V0	M5 GND	M6 V0	M7 GND	M8 V0	M9 GND	M10 V0	M11 GND	M12 V0	M13 GND	M14 V1	M15 GND	M16 V1	M17 GND	M18 V1	M19 GND	M20 V1	M21 GND	M22 V1	M23 OVDD	M24 SRIN0
L	L1 SROUT0	L2 ADOUT3	L3 GND	L4 OVDD	L5 V0	L6 GND	L7 V0	L8 GND	L9 V0	L10 GND	L11 V0	L12 GND	L13 V1	L14 GND	L15 V1	L16 GND	L17 V1	L18 GND	L19 V1	L20 V1	L21 V1	L22 GND	L23 SRIN1	L24 ADIN8
K	K1 GND	K2 ADOUT6	K3 ADOUT5	K4 GND	K5 OVDD	K6 V0	K7 GND	K8 V0	K9 GND	K10 V0	K11 GND	K12 V0	K13 GND	K14 V1	K15 GND	K16 V1	K17 GND	K18 V1	K19 GND	K20 OVDD	K21 GND	K22 ADIN6	K23 SRIN1	K24 GND
J	J1 ADOUT8	J2 ADOUT2	J3 OVDD	J4 GND	J5 V0	J6 GND	J7 V0	J8 GND	J9 V0	J10 GND	J11 V0	J12 GND	J13 V0	J14 GND	J15 V1	J16 GND	J17 V1	J18 GND	J19 V1	J20 GND	J21 OVDD	J22 GND	J23 ADIN7	J24 ADIN2
H	H1 SROUT1	H2 GND	H3 ADOUT7	H4 GND	H5 OVDD	H6 V0	H7 GND	H8 V0	H9 GND	H10 V0	H11 GND	H12 V0	H13 GND	H14 V1	H15 GND	H16 V1	H17 GND	H18 V1	H19 GND	H20 V0	H21 GND	H22 ADIN3	H23 ADIN0	H24 OVDD
G	G1 SROUT1	G2 GND	G3 ADOUT1	G4 GND	G5 GND	G6 GND	G7 V0	G8 GND	G9 V0	G10 GND	G11 V0	G12 GND	G13 V0	G14 OVDD	G15 V1	G16 GND	G17 V1	G18 GND	G19 V1	G20 OVDD	G21 V0	G22 V1	G23 ADIN1	G24 ADIN13
F	F1 ADOUT10	F2 OVDD	F3 ADOUT13	F4 OVDD	F5 V0	F6 OVDD	F7 GND	F8 V0	F9 OVDD	F10 V0	F11 GND	F12 SYSCLK	F13 GND	F14 V0	F15 GND	F16 OVDD	F17 V1	F18 V0	F19 OVDD	F20 GND	F21 GND	F22 OVDD	F23 ADIN14	F24 GND
E	E1 ADOUT12	E2 GND	E3 ADOUT9	E4 ADOUT32	E5 ADOUT21	E6 OVDD	E7 ADOUT23	E8 ADOUT39	E9 ADOUT18	E10 ADOUT15	E11 OVDD	E12 SYSCLK	E13 I2CGO	E14 OVDD	E15 ADIN18	E16 ADIN29	E17 ADIN30	E18 GND	E19 ADIN32	E20 ADIN31	E21 ADIN21	E22 ADIN9	E23 GND	E24 ADIN11
D	D1 CLKOUT	D2 CLKOUT	D3 ADOUT11	D4 ADOUT31	D5 GND	D6 ADOUT36	D7 ADOUT35	D8 OVDD	D9 ADOUT41	D10 ADOUT16	D11 GND	D12 BUS_CFG1	D13 PLLTEST	D14 GND	D15 ADIN15	D16 OVDD	D17 ADIN35	D18 ADIN27	D19 OVDD	D20 GND	D21 ADIN23	D22 OVDD	D23 ADIN10	D24 OVDD
C	C1 ADOUT26	C2 OVDD	C3 ADOUT25	C4 OVDD	C5 ADOUT33	C6 ADOUT27	C7 ADOUT14	C8 GND	C9 ADOUT40	C10 ADOUT28	C11 OVDD	C12 PLLTESTOUT	C13 OVDD	C14 ADIN28	C15 ADIN40	C16 ADIN19	C17 ADIN42	C18 ADIN43	C19 ADIN34	C20 ADIN33	C21 ADIN20	C22 ADIN22	C23 GND	C24 CLKIN
B	B1 GND	B2 ADOUT20	B3 GND	B4 ADOUT37	B5 ADOUT30	B6 ADOUT43	B7 OVDD	B8 ADOUT19	B9 ADOUT17	B10 GND	B11 BUS_CFG2	B12 EI_DISABLE	B13 KELV_GND2	B14 ADIN4	B15 ADIN16	B16 OVDD	B17 GND	B18 ADIN39	B19 OVDD	B20 ADIN36	B21 OVDD	B22 ADIN24	B23 ADIN25	B24 CLKIN
A		A2 ADOUT22	A3 OVDD	A4 ADOUT24	A5 GND	A6 ADOUT34	A7 ADOUT42	A8 ADOUT38	A9 ADOUT29	A10 KELV_OVDD	A11 BUS_CFG0	A12 AVDD	A13 ANALOGGND	A14 GND	A15 ADIN5	A16 ADIN17	A17 ADIN41	A18 ADIN26	A19 ADIN38	A20 GND	A21 ADIN37	A22 GND	A23 ADIN12	A24 OVDD

4.3 PowerPC 970MP Microprocessor Pinout Listings

Table 4-4 provides the pinout listing for the CBGA package.

Table 4-4. Pinout Listing for the CBGA Package (Page 1 of 6)

Signal Name	Pin Number	Active	I/O PI/PO[1]	Notes
ADIN(0:43)	H23, G23, J24, H22, B14, A15, K22, J23, L24, E22, D23, E24, A23, G24, F23, D15, B15, A16, E15, C16, C21, E21, C22, D21, B22, B23, A18, D18, C14, E16, E17, E20, E19, C20, C19, D17, B20, A21, A19, B18, C15, A17, C17, C18	—	Processor Input	—
ADOUT(0:43)	N2, G3, J2, L2, M2, K3, K2, H3, J1, E3, F1, D3, E1, F3, C7, E10, D10, B9, E9, B8, B2, E5, A2, E7, A4, C3, C1, C6, C10, A9, B5, D4, E4, C5, A6, D7, D6, B4, A8, E8, C9, D9, A7, B6	—	Processor Output	—
ANALOG_GND	A13	—	Analog GND	—
ATTENTION	AC7	High	Output	—
AV_{DD}	A12	—	Analog V_{DD}	—
$\overline{\text{AVP\_RESET}}$	U24	Low	Input	—
$\overline{\text{BI\_MODE}}$	AD24	Low	Input	—
BUS_CFG(0:2)	A11, D12, B11	—	Input	2
$\overline{\text{BYPASS}}$	T24	Low	Input	—
C1_UND_GLOBAL	AB17	High	Input	—
C2_UND_GLOBAL	AB15	High	Input	—
$\overline{\text{CHKSTOP}}$	T22	Low	OD BiDi	—
CKTERM_DIS	Y5	High	Input	—
CLKIN	C24	—	Processor Input	—
$\overline{\text{CLKIN}}$	B24	—	Processor Input	—
CLKOUT	D2	—	Processor Output	—
$\overline{\text{CLKOUT}}$	D1	—	Processor Output	—
CP0_DIODE_NEG	Y4	—	—	—
CP0_DIODE_POS	Y3	—	—	—
CP0_FRED_EN	Y11	High	Input	—
CP0_FRED_GND	AC12	—	GND	—
$\overline{\text{CP0\_HRESET}}$	AA9	Low	Input	—

Notes:

1. PI = processor input, PO= processor output, BiDi = bidirectional, OD = open drain. For additional information, see *Section 3.5 Processor Interconnect Specifications* on page 30.
2. The PLL_MULT and PLL_RANGE (1:0) bits can be overwritten by the JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They *must not* be connected to the GND and V_{DD} planes. See *Section 5.4.1 Using the Kelvin Voltage and Ground Pins* on page 61 and *Table 3-2 Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)* on page 23 for more details.
4. For correct operation, this pin must be tied to GND. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 4-4. Pinout Listing for the CBGA Package (Page 2 of 6)

Signal Name	Pin Number	Active	I/O PI/PO[1]	Notes
$\overline{\text{CP0\_INT}}$	AB13	Low	Input	—
CP0_KELV_GND0	W2	—	GND Test Points	3
CP0_KELV_V0	AB4	—	V_{DD} Test Points	3
CP0_PSRO0	V3	—	Output	—
$\overline{\text{CP0\_QACK}}$	AD21	Low	Input	—
$\overline{\text{CP0\_QREQ}}$	AB9	Low	Output	—
$\overline{\text{CP0\_SRESET}}$	AB7	Low	Input	—
CP1_DIODE_NEG	AC24	—	—	—
CP1_DIODE_POS	AB24	—	—	—
CP1_FRED_EN	AD17	High	Input	—
CP1_FRED_GND	Y12	—	GND	—
$\overline{\text{CP1\_HRESET}}$	AC16	Low	Input	—
$\overline{\text{CP1\_INT}}$	AD20	Low	Input	—
CP1_KELV_GND1	W22	—	GND Test Points	3
CP1_KELV_V1	W21	—	V_{DD} Test Points	3
$\overline{\text{CP1\_QACK}}$	AD18	Low	Input	—
$\overline{\text{CP1\_QREQ}}$	AC21	Low	Output	—
$\overline{\text{CP1\_SRESET}}$	AB22	Low	Input	—
$\overline{\text{DI2}}$	R24	Low	Input	—
EI_DISABLE	B12	High	Input	—

Notes:

1. PI = processor input, PO= processor output, BiDi = bidirectional, OD = open drain. For additional information, see *Section 3.5 Processor Interconnect Specifications* on page 30.
2. The PLL_MULT and PLL_RANGE (1:0) bits can be overwritten by the JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They *must not* be connected to the GND and V_{DD} planes. See *Section 5.4.1 Using the Kelvin Voltage and Ground Pins* on page 61 and *Table 3-2 Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)* on page 23 for more details.
4. For correct operation, this pin must be tied to GND. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 4-4. Pinout Listing for the CBGA Package (Page 3 of 6)

Signal Name	Pin Number	Active	I/O PI/PO[1]	Notes
GND	A5, A14, A20, A22 B1, B3, B10, B17 C8, C23 D5, D11, D14, D20 E2, E18, E23 F7, F11, F13, F15, F20, F21, F24 G2, G4, G5, G6, G8, G10, G12, G16, G18 H2, H4, H7, H9, H11, H13, H15, H17, H19, H21 J4, J6, J8, J10, J12, J14, J16, J18, J20, J22 K1, K4, K7, K9, K11, K13, K15, K17, K19, K21, K24 L3, L6, L8, L10, L12, L14, L16, L18, L22 M5, M7, M9, M11, M13, M15, M17, M19, M21 N3, N4, N6, N8, N10, N12, N14, N16, N18, N20 P2, P5, P7, P9, P11, P13, P15, P17, P19, P21, P23, P24 R1, R4, R6, R8, R10, R12, R14, R16, R18, R20, R23 T5, T7, T9, T11, T13, T15, T17, T19, T21 U4, U6, U8, U10, U12, U14, U16, U18, U20 V5, V7, V9, V11, V13, V15, V17, V19, V21, V23 W1, W3, W6, W8, W10, W12, W16, W18, W20 Y7, Y9, Y13, Y15, Y17, Y19, Y22 AA1, AA2, AA6, AA8, AA10, AA12, AA14, AA16, AA18, AA20, AA24 AB2, AB5, AB19 AC1, AC8, AC10, AC11, AC18, AC22 AD2, AD5, AD12, AD14, AD16, AD19, AD23	—	GND	—
GPULDBG	Y24	High	Input	—
$\overline{\text{I2CCK}}$	V24	—	OD BiDi	—
$\overline{\text{I2CDT}}$	V22	—	OD BiDi	—
I2CGO	E13	—	OD	—
I2CSEL	U1	High	Input	
KELV_GND2	B13	—	GND Test Points	3
KELV_OVDD	A10	—	OV_{DD} Test Points	3
LSSDMODE	U2	High	Input	—
LSSD_RAMSTOP_ENABLE	T2	High	Input	—

Notes:

1. PI = processor input, PO= processor output, BiDi = bidirectional, OD = open drain. For additional information, see *Section 3.5 Processor Interconnect Specifications* on page 30.
2. The PLL_MULT and PLL_RANGE (1:0) bits can be overwritten by the JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They *must not* be connected to the GND and V_{DD} planes. See *Section 5.4.1 Using the Kelvin Voltage and Ground Pins* on page 61 and *Table 3-2 Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)* on page 23 for more details.
4. For correct operation, this pin must be tied to GND. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 4-4. Pinout Listing for the CBGA Package (Page 4 of 6)

Signal Name	Pin Number	Active	I/O PI/PO[1]	Notes
LSSD_SCAN_ENABLE	U22	High	Input	—
LSSD_STOP_ENABLE	AC14	High	Input	—
LSSD_STOPC2_ENABLE	AB11	High	Input	—
LSSD_STOP_C2STAR_ENABLE	U3	High	Input	—
MASTERSEL	R2	—	Input	—
$\overline{\text{MCP}}$	AA21	Low	Input	—
PLL_LOCK	U23	High	Output	—
PLL_MULT	AC5	—	Input	2
PLL_RANGE(1:0)	AD3, AA4	—	Input	2
PLLTEST	D13	High	Input	—
PLLTESTOUT	C12	—	Output	—
PROCID(0:1)	N21, N22	—	Input	—
PSRO_ENABLE	Y21	—	Input	—
PSYNC	P4	—	Input	—
PULSE_SEL(0:2)	V1, T3, AD10	—	Input	—
$\overline{\text{RI}}$	W4	Low	Input	—
SPARE1	AD6	—	Input/Output	4
SPARE2	AC3	—	Input/Output	4
SRIN(0:1)	N24, K23	—	Processor Input	—
$\overline{\text{SRIN}}$(0:1)	M24, L23	—	Processor Input	—
SROUT(0:1)	M1, H1	—	Processor Output	—
$\overline{\text{SROUT}}$(0:1)	L1, G1	—	Processor Output	—
$\overline{\text{SYNC\_ENABLE}}$	W24	Low	Input	—
SYSCLK	F12	—	Input	—
$\overline{\text{SYSCLK}}$	E12	—	Input	—
TBEN	AD15	High	Input	—
TCK	AB23	—	Input	—
TDI	AA23	—	Input	—
TDO	AD8	—	Output	—

Notes:

1. PI = processor input, PO= processor output, BiDi = bidirectional, OD = open drain. For additional information, see *Section 3.5 Processor Interconnect Specifications* on page 30.
2. The PLL_MULT and PLL_RANGE (1:0) bits can be overwritten by the JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They *must not* be connected to the GND and V_{DD} planes. See *Section 5.4.1 Using the Kelvin Voltage and Ground Pins* on page 61 and *Table 3-2 Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)* on page 23 for more details.
4. For correct operation, this pin must be tied to GND. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 4-4. Pinout Listing for the CBGA Package (Page 5 of 6)

Signal Name	Pin Number	Active	I/O PI/PO[1]	Notes
TMS	AD22	—	Input	—
TRIGGEROUT	R22	High	Output	—
$\overline{\text{TRST}}$	AA13	Low	Input	—
V0	F5, F8, F10, F14, F18 G7, G9, G11, G13, G21 H6, H8, H10, H12, H20 J5, J7, J9, J11, J13 K6, K8, K10, K12 L5, L7, L9, L11 M4, M6, M8, M10, M12 N5, N7, N9, N11 P6, P8, P10, P12 R3, R5, R7, R9, R11 T1, T4, T6, T8, T10, T12 U5, U7, U9, U11 V2, V4, V6, V8, V10, V12 W5, W7, W9, W13 Y2, Y6, Y8 AA3, AA5, AA7, AA11 AB3, AB6, AB10 AC4, AC6 AD7, AD9, AD11	—	V_{DD}	—

Notes:

1. PI = processor input, PO= processor output, BiDi = bidirectional, OD = open drain. For additional information, see *Section 3.5 Processor Interconnect Specifications* on page 30.
2. The PLL_MULT and PLL_RANGE (1:0) bits can be overwritten by the JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They *must not* be connected to the GND and V_{DD} planes. See *Section 5.4.1 Using the Kelvin Voltage and Ground Pins* on page 61 and *Table 3-2 Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)* on page 23 for more details.
4. For correct operation, this pin must be tied to GND. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 4-4. Pinout Listing for the CBGA Package (Page 6 of 6)

Signal Name	Pin Number	Active	I/O PI/PO[1]	Notes
V1	F17 G15, G17, G19, G22 H14, H16, H18 J15, J17, J19 K14, K16, K18 L13, L15, L17, L19, L20, L21 M14, M16, M18, M20, M22 N13, N15, N17, N19, N23 P14, P16, P18, P20, P22 R13, R15, R17, R19, R21 T14, T16, T18, T20 U13, U15, U17, U19, U21 V14, V16, V18, V20 W15, W17, W19 Y14, Y16, Y18, Y20, Y23, AA15, AA17, AA19, AA22 AB12, AB14, AB16, AB18, AB20, AB21 AC15, AC19 AD13	—	V_{DD}	—
V2	A3, A24 B7, B16, B19, B21 C2, C4, C11, C13 D8, D16, D19, D22, D24 E6, E11, E14 F2, F4, F6, F9, F16, F19, F22 G14, G20 H5, H24 J3, J21 K5, K20 L4 M3, M23 N1 T23 W11, W14, W23 Y1, Y10 AB1, AB8 AC2, AC9, AC13, AC17, AC20, AC23 AD1, AD4	—	OV_{DD}	—
Z_OUT	P3	—	—	4
Z_SENSE	P1	—	—	4

Notes:

1. PI = processor input, PO= processor output, BiDi = bidirectional, OD = open drain. For additional information, see *Section 3.5 Processor Interconnect Specifications* on page 30.
2. The PLL_MULT and PLL_RANGE (1:0) bits can be overwritten by the JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands during the power-on reset (POR) sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
3. These pins should be used as regulator references and also to measure on-chip voltage drop and noise. They *must not* be connected to the GND and V_{DD} planes. See *Section 5.4.1 Using the Kelvin Voltage and Ground Pins* on page 61 and *Table 3-2 Maximum Allowable Current on Kelvin Probe Pins (DD1.1x)* on page 23 for more details.
4. For correct operation, this pin must be tied to GND. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

5. System Design Information

This section provides electrical and thermal design recommendations for the successful application of the PowerPC 970MP.

5.1 External Resistors

The PowerPC 970MP contains no internal pull-up resistors for any Joint Test Action Group (JTAG), I^2C, mode select, or asynchronous inputs. System designs must include these external resistors where required. See *Table 5-7 PowerPC 970MP Debug and Bringup Pin Settings and Information* on page 64, *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65, and *Section 3.10.3 I^2C and JTAG Considerations* on page 43 for information about implementing external pullups and pulldowns.

5.2 Phase-Locked Loop Configuration

This section helps the user configure the phase-locked loop (PLL) and determine SYSCLK input frequency for PowerPC 970MP systems.

Note: For applications using external termination resistors on SYSCLK and $\overline{\text{SYSCLK}}$, CKTERM_DIS should be pulled up to OV_{DD} to disable the internal termination. To use the internal 50 Ω parallel termination, CKTERM_DIS should be pulled to GND to avoid problems with the PLL lock.

5.2.1 Determining PLLMULT and BUS_CFG Settings

The first step is to determine the bus frequency. This parameter is a critical component of overall system performance. The bus should run as fast as your memory controller and bridge chip can support. Once you have determined your maximum bus frequency, select a bus multiplier ratio that will deliver the optimal processor core frequency.

Note: The PLL_MULT and PLL_RANGE bits can be overwritten by JTAG commands, and the BUS_CFG bits can be changed by scan communication (SCOM) commands, during the power-on reset (POR) sequence. These overrides are cleared after every $\overline{\text{HRESET}}$. See the *PowerPC 970MP Power-On Reset Application Note* for more details.

Table 5-1 PowerPC 970MP Bus Configuration on page 58 shows the available bus ratios. In most applications, this would be the highest frequency possible for a given PowerPC 970MP part number, but other considerations (for example, available power) might take precedence.

Table 5-1. PowerPC 970MP Bus Configuration

BUS_CFG(0:2)	Ratio	Notes
000	2:1	
001	3:1	
010	4:1	1
011	6:1	1
100	8:1	2
101	12:1	3
110	24:1	2
111	Not valid	

Note: BUS_CFG bits can be changed by SCOM commands during the POR sequence. See the *PowerPC 970MP RISC Microprocessor Design Guide* and the *PowerPC 970MP Power-On Reset Application Note*.

1. Limited power-tuning frequency scaling.
2. Bus ratios of 8:1 and 24:1 are not supported for processor input (PI) functionality and power tuning.
3. No power-tuning frequency scaling.

The bus frequency multiplier ratio typically indicates the desired PLL multiplier setting. Ratios based on multiples of 3 (3:1, 6:1, 12:1) should always use PLLMULT = ‘0’ (low) for a PLL multiplier of 12. The required core frequency should be divided by 12 to determine the required input SYSCLK frequency. Ratios based on multiples of 2 (2:1, 4:1, 8:1, 24:1) should always use PLLMULT = ‘1’ (high) to multiply SYSCLK by 8.

Note: Using bus frequency ratios of 3:1, 6:1 or 12:1 with PLLMULT = ‘1’ or ratios of 8:1 or 24:1 with PLLMULT = ‘0’ is not recommended. Internal clock synchronization delays might reduce performance.

After the correct BUS_CFG(0:2) and PLL_MULT pin settings are determined, the required SYSCLK input frequency can be determined. The selected SYSCLK input frequency should be within the minimum and maximum frequencies specified in *Table 3-8 Clock ac Timing Specifications* on page 27.

5.2.2 PLL_RANGE Configuration

Table 5-2 shows the PLL voltage controlled oscillator (VCO) configuration for the PowerPC 970MP, using the pins PLL_RANGE1 and PLL_RANGE0.

Table 5-2. PowerPC 970MP PLL Configuration

PLL_RANGE(1:0) Settings			
Range Name	PLL_RANGE1	PLL_RANGE0	Frequency Range
Low	0	0	Frequency < 1.2 GHz
Medium	0	1	1.2 GHz ≤ Frequency < 1.6 GHz
High	1	0	1.6 GHz ≤ Frequency
Reserved	1	1	Reserved

Notes:

1. The PLL_MULT and PLL_RANGE(1:0) bits can be overwritten by JTAG commands, and the BUS_CFG bits can be changed by SCOM commands, during the POR sequence. See the *PowerPC 970MP Power-On Reset Application Note* for more details.
2. PLL frequency range settings are not an indicator of available PowerPC 970MP processor speeds.

5.3 PLL Power Supply Filtering

The PowerPC 970MP microprocessor has a separate pin, AV_{DD}, that provides power to the clock generation PLL.

To ensure stability of the internal clock, filter the AV_{DD} power and ANALOG_GND supplied to the PLL using a circuit similar to *Figure 5-1*. To ensure that the capacitor filters out as much noise as possible, the capacitor should be placed as close as possible to the AV_{DD} and ANALOG_GND pins. The capacitor used should have minimal inductance. The ferrite bead shown in *Figure 5-1* should supply an impedance of less than 70 Ω in the 100 - 500 MHz region. It is recommended that the ferrite bead be placed within 1.5 cm, preferably closer, to the AV_{DD} pin.

The intent of all the recommendations it to provide a low noise voltage input to the PLL circuit. Place the filter close to the pins. Close proximity of the filter to the pins, as well as It is also critical to avoid coupling to nearby traces, both on the same plane and internal layers, especially after the filter is critical.

Note: AV_{DD} measured at the pins of the part should never be more than 50 mV lower than the AV_{DD} voltage range specified in *Table 3-3 Recommended Operating Conditions* on page 24.

Figure 5-1. PLL Power Supply Filter Circuit

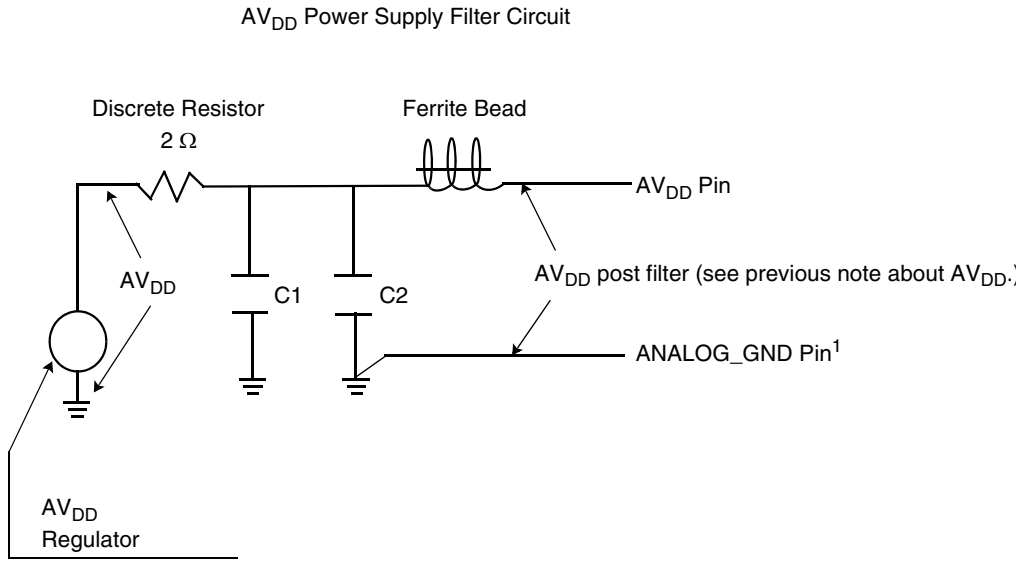


Table 5-3. Filter Components

Item	Description/Value
Resistor	2 Ω
C1	0.1 µF X7F
C2	10.0 µF YV5
Ferrite Bead	Murata BLM21PG300SN1 or similar

Notes:
1. Connected to analog ground without a filter.

5.4 Decoupling Recommendations

Capacitor decoupling is required for the PowerPC 970MP. Decoupling capacitors act to reduce medium-frequency and high-frequency chip switching noise and to provide localized bulk charge storage to reduce major power surge effects. Recommendations for medium-frequency and high-frequency noise decoupling are provided. Bulk decoupling requires a more complete understanding of the system and system power architecture, and is beyond the scope of this document.

High-frequency decoupling capacitors should be located as close as possible to the processor with low lead inductance to the ground and voltage planes. The recommended placement of the decoupling capacitors is shown in *Figure 5-2 Decoupling Capacitor Locations (Preliminary)* on page 63.

The decoupling capacitors in the center of the module, directly under the chip, are particularly effective in medium-frequency and high-frequency noise reduction. Capacitance in this region should be maximized, while inductive parasitics are minimized. To achieve this, the recommended capacitor layout uses as many V0 to GND and V1 to GND capacitors as possible in this region.

Table 5-4. Recommended Decoupling Capacitor Specifications

Specification	Value
Size	0402 (1.00 mm × 0.50 mm)
Capacitance	220 nF
Dielectric type	Y5V or X7R
Voltage rating	6 V

Table 5-5. Recommended Minimum Number of Decoupling Capacitors

Category	Minimum Number
Minimum decoupling capacitors	150 total
Minimum V0 - GND	67
Minimum V1 - GND	66
Minimum OV_{DD} - GND	17 OV_{DD}
Note: Add additional decoupling capacitors to improve noise performance.	

5.4.1 Using the Kelvin Voltage and Ground Pins

The PowerPC 970MP features three pairs of Kelvin voltage and GND pins to assist in analyzing on-chip noise and voltage drop. Pins CP0_KELV_V0 and CP0_KELV_GND0 are the V0 to GND pair. Pins CP1_KELV_V1 and CP1_KELV_GND1 are the V1 to GND pair. Pins KELV_OVDD and KELV_GND2 are the OV_{DD} to GND pair.

Table 3-2 on page 23 defines the maximum current allowed on the Kelvin pins. Exceeding these maximum currents can cause permanent damage to the microprocessor. Oscilloscope probes should provide enough impedance to prevent excess current on these pins.

Caution: The Kelvin ground and Kelvin voltage pins should never be connected into the normal voltage or GND planes. If a Kelvin pin is not in use, it requires a high impedance termination so that the current limits on the pins are not exceeded.

These pins should be brought out to test pads by traces that are as short as possible. An oscilloscope can be used on these test pads to measure on-chip voltage noise and to verify the decoupling and voltage regulation in a design.

It is recommended that the voltage difference between CP0_KELV_V0 and CP0_KELV_GND0 be used to sense the voltage of the V0 voltage regulators, and that the voltage difference between CP1_KELV_V1 and CP0_KELV_GND1 be used to sense the voltage of the V1 voltage regulators. If both V0 and V1 share the same power plane, the CP0_KELV_V0 and CP0_KELV_GND0 pins should be used as the voltage sense (Vsense) of the voltage regulator. The KELV_V and KELV_GND pins used should be connected to the differential inputs of a suitable operational amplifier to limit current on those pins and also to provide some common mode noise rejection. The output of this operational amplifier is used as the Vsense of the voltage regulator.

This voltage sensing signal must be sufficiently filtered to ensure that the tracking supply is not modulated by switching noise generated within the processor. This filtering is required to maintain stable regulation. The configuration and degree of filtering required depends upon the response time and tracking accuracy of the power supplies, and the dynamics of application-induced load changes.

5.4.2 Power Supply Sequencing and Ramping

The PowerPC 970MP power supplies can be ramped in any order providing that all supplies are stable and within the allowable tolerance within 2 seconds. The V1 supply is independent of any other supply rail during power-up or power-down. However, when both V0 and V1 are powered, V0 and V1 should be regulated within 150 mV of each other.

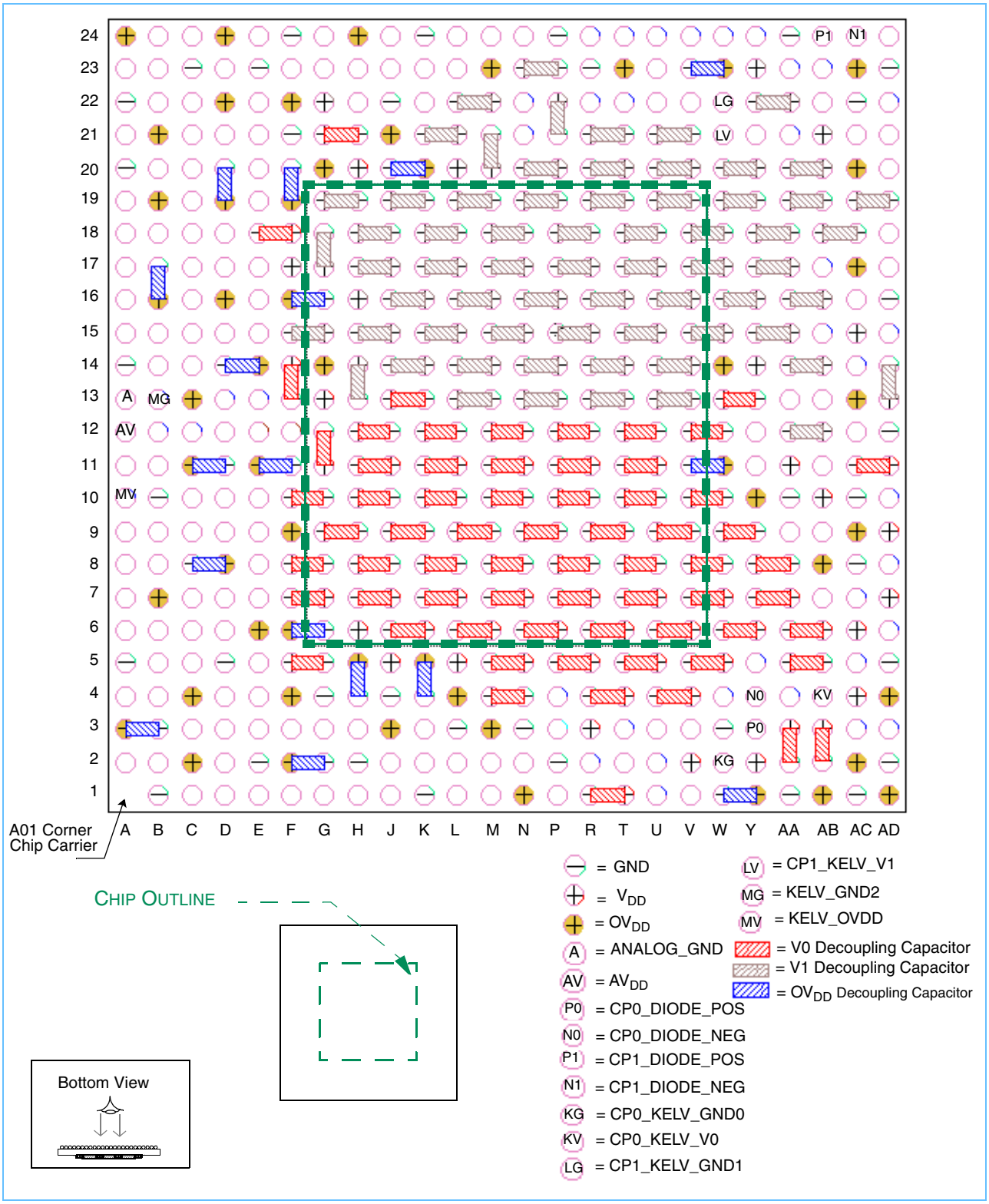
The maximum voltage differences during operation and while ramping must be maintained according to *Table 5-6*.

Table 5-6. Maximum Voltage Difference Between Supply Rails

Supply Rails	Maximum Difference During Operation (After 2-Second Ramp Time)	Maximum Difference While Ramping (First 2 Seconds)
V0 : OV_{DD}	0.8 V	1.55 V
V0 : V1	150 mV	
V0 : AV_{DD}	2.5 V	2.75 V

5.5 Decoupling Layout Guide

Figure 5-2. Decoupling Capacitor Locations (Preliminary)



5.6 Pullup and Pulldown Recommendations

For reliable operation, it is highly recommended that the unused inputs be connected to an appropriate signal level. For example:

- Unused active-low inputs should be pulled up to OV_{DD}.
- Multiple unused active-high inputs can be ganged together for convenience.
- Unused active-high inputs should be connected to GND.
- Multiple unused active-low inputs can be ganged together for convenience.
- All no-connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V0, V1, OV_{DD}, AV_{DD}, ANALOG_GND, and GND pins of the PowerPC 970MP.

Table 5-7 provides details about the pin settings and information of the PowerPC 970MP debug and bringup signals. *Table 5-8* on page 65 provides details about the appropriate connections for the PowerPC 970MP manufacturing-test-only signals.

Table 5-7. PowerPC 970MP Debug and Bringup Pin Settings and Information

Pin Name	In/Out/BiDi/JTAG[1]	Pull-up and Pull-Down Resistor Setting[2]	Comments	Notes
$\overline{\text{AVP\_RESET}}$	In	Up		
C1_UND_GLOBAL	In	Down		
C2_UND_GLOBAL	In	Down		
GPULDBG	In	Up		3
I2CGO	OD	Up	Semaphore providing arbitration between I^2C and JTAG.	
I2CSEL	In	—	Allows external selection of the I^2C or JTAG interface for controlling scan functionality.	4, 5
TCK	In-JTAG	Up	JTAG – test clock	4
TDI	In-JTAG	Up	JTAG – test data in	4
TDO	Out-JTAG	Up	JTAG – test data out	4
TMS	In-JTAG	Up	JTAG – test mode select	4
TRIGGEROUT	Out	Down	Make visible to external hardware.	
$\overline{\text{TRST}}$	In-JTAG	Up	Only needed for debug. $\overline{\text{HRESET}}$ performs the common on-chip processor (COP) reset function. Should be wired to the debug connector. Pulled up to OV_{DD} by a 10 kΩ resistor.	

1. BiDi = Bidirectional.
2. Pullups should use a 10 kΩ resistor to OV_{DD}. Pulldowns should use a 10 kΩ resistor to GND.
3. If GPULDBG = '1' during $\overline{\text{HRESET}}$ transition from low to high, then run power-on reset (POR) in debug mode and stop after each POR instruction.
   If GPULDBG = '0' during $\overline{\text{HRESET}}$ transition from low to high, then run POR without stopping after each POR instruction. Toggling GPULDBG from '1' to '0' later on will exit the POR debug mode and continue without stopping after each instruction. See the *PowerPC 970MP Power-On Reset Application Note.* for more information.
4. For I^2C operation. See *Section 3.10.3 I^2C and JTAG Considerations* on page 43.
5. Pull-up and pull-down settings are application dependent. See *Section 3.10.3 I^2C and JTAG Considerations* on page 43.

Table 5-8. PowerPC 970MP Pins for Manufacturing Test Only

Pin Name	Signal Direction	Pullup or Pulldown	Notes
$\overline{\text{BI\_MODE}}$	In	Up	1
CP0_FRED_EN	In	Down	2
CP1_FRED_EN	In	Down	2
$\overline{\text{DI2}}$	In	Up	1
LSSDMODE	In	Down	2
LSSD_RAMSTOP_ENABLE	In	Down	2
LSSD_SCAN_ENABLE	In	Down	2
LSSD_STOPC2_ENABLE	In	Down	2
LSSD_STOP_C2STAR_ENABLE	In	Down	2
LSSD_STOP_ENABLE	In	Down	2
PLLTEST	In	Down	2
PSRO_ENABLE	In	Down	—
CP0_PSRO0	Out	NC	—
PULSE_SEL(0:2)	In	Down	2
$\overline{\text{RI}}$	In	Up	1
SPARE1	In/Out	—	3
SPARE2	In/Out	—	3
$\overline{\text{SYNC\_ENABLE}}$	In	Down	2
Z_OUT	—	—	3
Z_SENSE	—	—	3

Note:

1. Pullups should use a 10 kΩ resistor to OV_{DD}.
2. Pulldowns should use a 10 kΩ resistor to GND.
3. Should be tied to GND.

5.7 Input-Output Use

This section provides information about the PowerPC 970MP input and output signals and their use.

5.7.1 Chip Signal I/O and Test Pins

Table 5-9 shows the system signal names, debug pins, and test pins.

Table 5-9. Input/Output Signal Descriptions (Page 1 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
ADIN(0:43)	44	In	System: processor interface (PI) address or data and control information inputs.	—
ADOUT(0:43)	44	Out	System: PI address or data and control information outputs.	—
ATTENTION	1	Out	If asserted, the service processor should read the Joint Test Action Group (JTAG) register.	—
$\overline{\text{AVP\_RESET}}$	1	In	Manufacturing test use only.	—
$\overline{\text{BI\_MODE}}$	1	In	Manufacturing test use only.	—
$\overline{\text{BYPASS}}$	1	In	Used to bypass the phase-locked loop (PLL).	—
BUS_CFG(0:2)	3	In	These signals are used to select the bus frequency division factor from the processor clock of 2, 3, 4, 6, 8, 12, or 24. 000 2:1 001 3:1 010 4:1 011 6:1 100 8:1 101 12:1 110 24:1 111 invalid	1, 2, 3
C1_UND_GLOBAL	1	In	Debug: adjusts the C1 clock to internal latches, and is not used for normal operation.	—
C2_UND_GLOBAL	1	In	Debug: adjusts the C2 clock to internal latches, and is not used for normal operation.	—
$\overline{\text{CHKSTOP}}$	1	Open drain (OD) Bidirectional (BiDi)	System: checkstop input and output.	
CKTERM_DIS	1	In	Disables the 50 Ω parallel internal SYSCLK termination. Pulled up to OV_{DD} for applications that use external termination on SYSCLK and $\overline{\text{SYSCLK}}$. Otherwise, this signal is pulled low to GND.	—

Notes:

1. Bus ratios 8:1 and 24:1 are not supported for processor input (PI) functionality.
2. Using the 4:1 or 12:1 ratio with a multiplier of 12 limits the use of power tuning to (frequency)/2.
3. The PLL_MULT can be overwritten by JTAG commands. See the *PowerPC 970MP RISC Microprocessor Design Guide* or the *PowerPC 970MP User's Manual* for more details.
4. OD = open drain. BiDi = bidirectional.
5. For a PowerPC 970MP, MASTERSEL must be controlled by the service processor to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a PowerPC 970MP, MASTERSEL must always be set to low (including during the entire power-up sequence)
6. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 5-9. Input/Output Signal Descriptions (Page 2 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
CLKIN	1	In	System: PI clock in. This is a differential clock returned to the processor.	—
$\overline{\text{CLKIN}}$	1	In	System: PI clock in. This is a differential clock returned to the processor.	—
CLKOUT	1	Out	System: PI differential clock to the bus.	—
$\overline{\text{CLKOUT}}$	1	Out	System: PI differential clock to the bus.	—
CP0_FRED_EN	1	In	For manufacturing test use only.	—
CP1_FRED_EN	1	In	For manufacturing test use only.	—
$\overline{\text{DI2}}$	1	In	For manufacturing test use only.	—
EI_DISABLE	1	In	Debug: disables the use of the initial alignment procedure (IAP), which adjusts the clock skew on the processor interface.	—
GPULDBG	1	In	Debug: POR debug mode select.	—
$\overline{\text{CP0\_HRESET}}$	1	In	System: power-on reset for core 0.	—
$\overline{\text{CP1\_HRESET}}$	1	In	System: power-on reset for core 1.	—
$\overline{\text{I2CCK}}$	1	OD/Bidi	System: I^2C signal clock.	4
$\overline{\text{I2CDT}}$	1	OD/Bidi	System: I^2C interface data.	4
I2CGO	1	OD	Debug: semaphore signal to arbitrate JTAG or I^2C access.	—
I2CSEL	1	In	Debug: allows for the external selection of the I^2C or JTAG interface for controlling scan functionality.	—
$\overline{\text{CP0\_INT}}$	1	In	System: external interrupt for core 0 when low.	—
$\overline{\text{CP1\_INT}}$	1	In	System: external interrupt for core 1 when low.	—
LSSD_RAMSTOP_ENABLE	1	In	For manufacturing test use only.	—
LSSD_SCAN_ENABLE	1	In	For manufacturing test use only.	—
LSSD_STOP_ENABLE	1	In	For manufacturing test use only.	—
LSSD_STOPC2_ENABLE	1	In	For manufacturing test use only.	—
LSSD_STOPC2STAR_ENABLE	1	In	For manufacturing test use only.	—
LSSDMODE	1	In	For manufacturing test use only.	—
MASTERSEL	1	In	System: external selection of PU0 or PU1 as the master core.	5
$\overline{\text{MCP}}$	1	In	System: machine check interrupt.	—
PLL_LOCK	1	Out	Indicates that the phase-locked loop (PLL) has locked.	—

Notes:

1. Bus ratios 8:1 and 24:1 are not supported for processor input (PI) functionality.
2. Using the 4:1 or 12:1 ratio with a multiplier of 12 limits the use of power tuning to (frequency)/2.
3. The PLL_MULT can be overwritten by JTAG commands. See the *PowerPC 970MP RISC Microprocessor Design Guide* or the *PowerPC 970MP User's Manual* for more details.
4. OD = open drain. BiDi = bidirectional.
5. For a PowerPC 970MP, MASTERSEL must be controlled by the service processor to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a PowerPC 970MP, MASTERSEL must always be set to low (including during the entire power-up sequence)
6. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 5-9. Input/Output Signal Descriptions (Page 3 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
PLL_MULT	1	In	Selects PLL multiplication factor: 0 Multiply reference frequency by 12. 1 Multiply reference frequency by 8.	3
PLL_RANGE(1:0)	2	In	To select the PLL frequency range, see *Table 5-2 PowerPC 970MP PLL Configuration* on page 59.	—
PLLTEST	1	In	For manufacturing test use only.	—
PLLTESTOUT	1	Out	Measure the PLL output (divided by 64).	—
PROCID(0:1)	2	In	System: processor ID	—
PSRO_ENABLE	1	In	For manufacturing test use only.	—
CP0_PSRO0	1	Out	For manufacturing test use only.	—
PSYNC	1	In	System: phase synchronization with companion chip	—
PULSE_SEL(0:2)	3	In		—
$\overline{\text{CP0\_QACK}}$	1	In	System: acknowledgment of quiescence from the system for core 0.	—
$\overline{\text{CP1\_QACK}}$	1	In	System: acknowledgment of quiescence from the system for core 1.	—
$\overline{\text{CP0\_QREQ}}$	1	Out	System: request from processor to quiesce the system (nap mode).	
$\overline{\text{CP1\_QREQ}}$	1	Out	System: request from processor to quiesce the system (nap mode).	
$\overline{\text{RI}}$	1	In	For manufacturing test use only.	—
SPARE1	1	In/Out		6
SPARE2	1	In/Out		6
$\overline{\text{CP0\_SRESET}}$	1	In	System: soft reset for core 0.	—
$\overline{\text{CP1\_SRESET}}$	1	In	System: soft reset for core 1.	—
SRIN(0:1)	2	In	System: PI snoop response in.	—
$\overline{\text{SRIN}}$(0:1)	2	In	System: PI inverse of snoop response in.	—
SROUT(0:1)	2	Out	System: PI snoop response out.	—
$\overline{\text{SROUT}}$(0:1)	2	Out	System: PI inverse of snoop response out.	—
$\overline{\text{SYNC\_ENABLE}}$	1	In	For manufacturing test use only.	—
SYSCLK	1	In	System reference clock (differential input).	—
$\overline{\text{SYSCLK}}$	1	In	System reference clock (differential input).	—
TBEN	1	In	System: time base enable	—

Notes:

1. Bus ratios 8:1 and 24:1 are not supported for processor input (PI) functionality.
2. Using the 4:1 or 12:1 ratio with a multiplier of 12 limits the use of power tuning to (frequency)/2.
3. The PLL_MULT can be overwritten by JTAG commands. See the *PowerPC 970MP RISC Microprocessor Design Guide* or the *PowerPC 970MP User's Manual* for more details.
4. OD = open drain. BiDi = bidirectional.
5. For a PowerPC 970MP, MASTERSEL must be controlled by the service processor to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a PowerPC 970MP, MASTERSEL must always be set to low (including during the entire power-up sequence)
6. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

Table 5-9. Input/Output Signal Descriptions (Page 4 of 4)

Pin Name	Width	In/Out	System/Debug Function	Notes
TCK	1	In	JTAG: test clock that is separate from the system clock tree. Controls all test access port functions.	—
TDI	1	In	JTAG: serial input used to feed test data and test access port instructions.	—
TDO	1	Out	JTAG: serial output used to extract data from the chip under test control.	—
TMS	1	In	JTAG: test mode select used to control the operation of the JTAG state machine.	—
TRIGGEROUT	1	Out	Signal to indicate that internal trace collection has begun.	—
$\overline{\text{TRST}}$	1	In	JTAG: asynchronous reset for the JTAG state machine.	—

Notes:

1. Bus ratios 8:1 and 24:1 are not supported for processor input (PI) functionality.
2. Using the 4:1 or 12:1 ratio with a multiplier of 12 limits the use of power tuning to (frequency)/2.
3. The PLL_MULT can be overwritten by JTAG commands. See the *PowerPC 970MP RISC Microprocessor Design Guide* or the *PowerPC 970MP User's Manual* for more details.
4. OD = open drain. BiDi = bidirectional.
5. For a PowerPC 970MP, MASTERSEL must be controlled by the service processor to easily read the fuse string for each core. The fuse string is not to be read during normal operation. During normal operation of a PowerPC 970MP, MASTERSEL must always be set to low (including during the entire power-up sequence)
6. See *Table 5-8 PowerPC 970MP Pins for Manufacturing Test Only* on page 65.

5.8 Thermal Management Information

Each PowerPC 970MP processor features on-die temperature sensing diodes. *Figure 5-3* provides a schematic of the thermal diode. The PU0 diode is connected to pins CP0_DIODE_NEG (Y4) and CP0_DIODE_POS (Y3). The PU1 diode is connected to pins CP1_DIODE_NEG (AC24) and CP1_DIODE_POS (AB24). External circuitry should force a controlled 100 μA forward bias current through the diode and monitor the diode's voltage drop to determine on-chip junction temperature. The accuracy of this process depends on the external circuitry's measurement accuracy and resolution. Depending on the system accuracy requirements, board level calibration might be required once during manufacturing.

Section 5.9 Scanning Thermal Diode Calibration and V_{DD} Fuse Code Data on page 71 describes the process for determining processor junction temperature based upon these measurements.

Additional temperature sensors can be implemented with the PowerPC 970MP; they should be mounted as close to the PowerPC 970MP as practical. Any external temperature-sensing hardware should be considered secondary, supplemental, or backup; correlation with the on-die thermal diode sensors requires calibration or board level characterization and validation. If the junction temperature of the processor is at risk of exceeding the maximum limits of this specification, an immediate power management sequence or system shutdown should be initiated to mitigate serious reliability degradation or permanent damage to the processor.

Figure 5-3. Thermal Diode Schematic

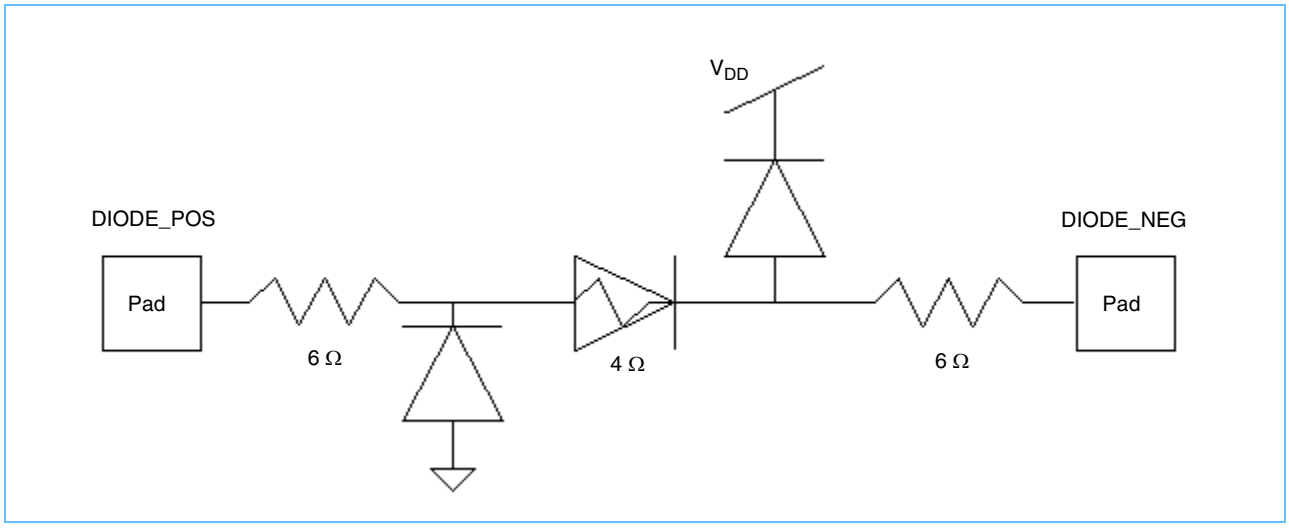
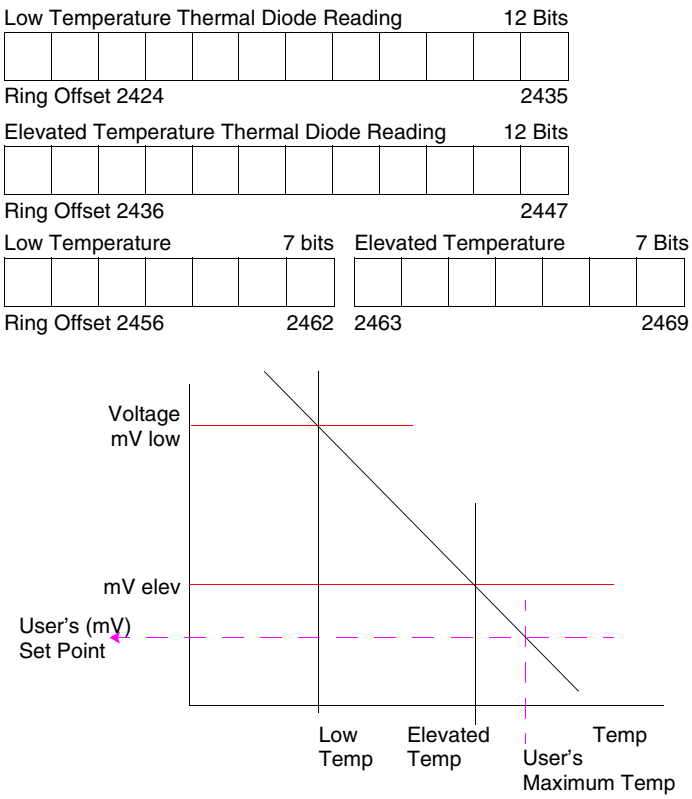


Figure 5-4 illustrates the PowerPC 970MP processor thermal diode implementation.

Figure 5-4. PowerPC 970MP Processor Thermal Diode Implementation



5.9 Scanning Thermal Diode Calibration and V_{DD} Fuse Code Data

Note: For correct fuse operation, make sure the SPARE1 and SPARE2 pins are tied to GND.

To access the thermal diode calibration data stored in each processor, a sequence of JTAG or I^2C commands must be issued. By using JTAG or I^2C commands, the desired data will appear serially on the PowerPC 970MP TDO pin or can be read using I^2C. For the PowerPC 970MP, this data must be read for each core.

This is a one-time only procedure. It is assumed the thermal diode calibration and V_{DD} fuse code (VFC) data stored in each processor is captured and stored in system read-only memory (ROM) for subsequent use. This procedure is not meant to be run at every system startup, because reading out this calibration data leaves the processor in an unusable state until it is restarted.

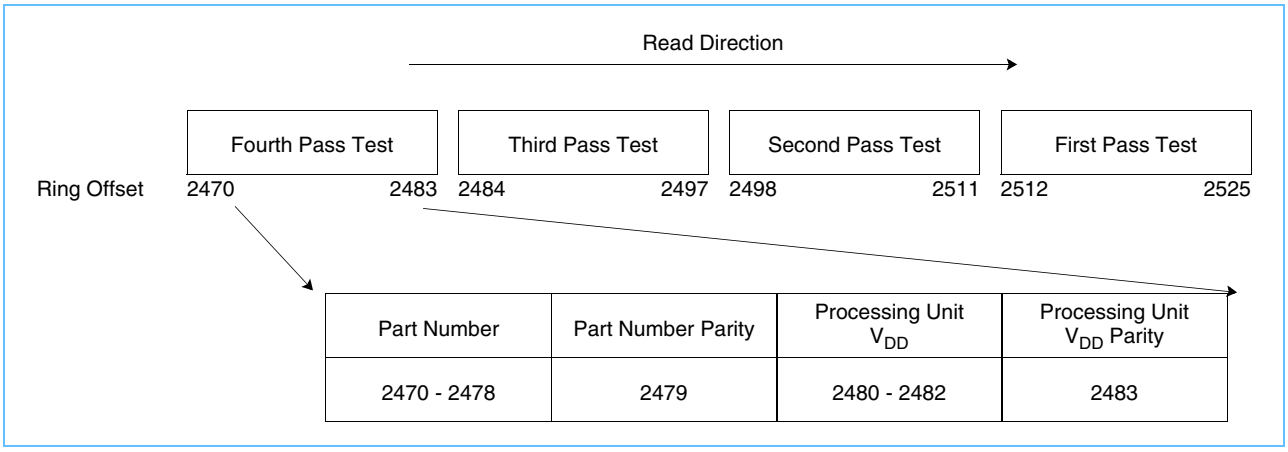
During the power-on reset (POR) sequence, the processor comes to a WAIT state to allow the service processor to scan the MODE ring facility. It is during this WAIT state that the thermal diode data can be scanned out. Scanning the MODE ring is not necessary. The *PowerPC 970MP Power-On Reset Application Note* provides much more detail about reading the fuse data.

5.9.1 VFC Fusing Implementation

Processing unit 0 and processing unit 1 are fused separately. The part number is represented by nine fused bits plus one parity bit. The voltage for the processing unit is represented by three fused bits plus one parity bit. Although there is VFC data for each processing unit, the values are the same on a per part basis

There are four possible locations for the VFC data. All 14 bits in the fourth pass test location should be read first. If zero, then read all 14 bits in the third pass test location. If zero, then read all 14 bits in the second pass test location. If zero, then read all 14 bits in the first pass test location. If zero, then the processor was not fused with VFC data; notify your IBM representative. The first detected test location with nonzero data should be decoded and no further test locations should be read. See *Figure 5-5* for more details about the PowerPC 970MP VFC data implementation.

Figure 5-5. PowerPC 970MP VFC Implementation



5.9.2 Booting Voltage

The maximum voltage for the specified processor frequency shown in *Table 3-7 PowerPC 970MP V0 and V1 V_{DD}* on page 26 must be used to boot the processor until the VFC data is read. This means that reading VFC data and setting the voltage regulator should be done as soon as possible after POR.

5.10 Heatsink Attachment and Mounting Forces

Table 5-10 and *Figure 5-6* describe the allowable forces for the PowerPC 970MP package. Heatsink design should not exceed these static or dynamic forces.

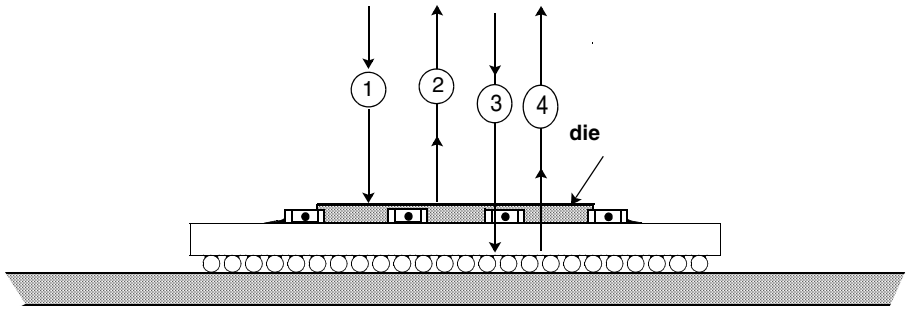
Table 5-10. Allowable Forces on the PowerPC 970MP Package

Callout Number	Characteristic		Symbol	Maximum	Unit[1]	Note
1	Compressive force on the die	Static	F_C	133.5	N	2
		Dynamic		133.5	N	2
2	Tensile force on the die	Static	F_T	530	N	2
		Dynamic		530	N	2
3	Compressive force on the ball grid array (BGA) balls	Static	F_{BGA}	90.3	N	
		Dynamic		113.0	N	3
4	Tensile force on the BGA balls	Static	F_T	0	N	
		Dynamic		17.6	N	

Note:

1. One newton = 0.2248089 pound-force.
2. Might be limited by the BGA limit.
3. The maximum force value for callout item 3 must include the force value for callout item 1.

Figure 5-6. Force Diagram for the PowerPC 970MP Package



Note: The legend for this figure is provided by callout number in *Table 5-10*.

5.11 Operational and Design Considerations

5.11.1 I^2C Addressing of the PowerPC 970MP

The I^2C address of PowerPC 970MP processor is specified by the binary value ‘1000ppc’ where “pp” equals the setting of the processor ID bits PROCID(0:1), and “c” identifies the core; c = ‘0’ for PU0, and c = ‘1’ for PU1. For example, if the PROCID bits are both set to ‘0’, the address for PU0 is ‘1000000’, and the address for PU1 is ‘1000001’. If the PROCID bits are set to ‘01’, the address for PU0 is ‘1000010’, and the address for PU1 is ‘1000011’, and so forth.