NOTE THAT THE RM7000C XYLINX PROM BINARY STRING IS LITTLE ENDIAN: 10000000 01010101 00000001 00000010
*CPU is fed these boot mode bits as bytes in little endian mode. 7 -> 0 15 -> 8 23 -> 16 32 -> 24

These values ABOVE are in the Xyinx, within the table itself these values are LSB -> MSB
Byte flipped from the above yields: 0 -> 7 8 -> 15 16 -> 23 24 -> 31
600MHz RM7000C mode bits: 00000001 10101010 10000000 01000000

NOTE: IN ORDER TO OBTAIN BOOT-MODE VALUES WHICH MAKE SENSE FOR THE 600MHZ CPU BYTE FLIPPING IS REQUIRED

Table 16 Boot Time Mode Stream

Mode bit	Description	Mode bit	Description
0 0	reserved (must be zero)	[17:16] 01	System configuration identifiers - software visible in ***Config[21:20]***
[4:1] 0000	Write-back data rate 0: DDDD 1: DDxDDx 2: DDxxDDxx 3: DxDxDxDx 4: DDxxxDDxxx 5: DDxxxxDDxxxx 6: DxxDxxDxxDxx 7: DDxxxxxxDDxxxxxx 8: DxxxDxxxDxxxDxxx 9-15: reserved	[19:18 00	Reserved: Must be zero
[7:5] 100	SysClock to Pclock Multiplier Mode bit 20 = 0 / Mode bit 20 = 1 0: Multiply by 2/x 1: Multiply by 3/x 2: Multiply by 4/x 3: Multiply by 5/2.5 4: Multiply by 6/x 5: Multiply by 7/3.5 6: Multiply by 8/x 7: Multiply by 9/4.5	20 0	Pclock to SysClock multipliers. 0: Integer multipliers (2,3,4,5,6,7,8,9) 1: Half integer multipliers (2.5,3.5,4.5)
8 0	Specifies byte ordering. Logically ORed with BigEndian input signal. 0: Little endian 1: Big endian	[23:21] 00	Reserved: Must be zero
[10:9] 1 0	Non-Block Write Control 00: R4000 compatible non-block writes 01: reserved 10: pipelined non-block writes 11: non-block write re-issue	24 0	JTLB Size. 0: 48 dual-entry 1: 64 dual-entry
11 0	Timer Interrupt Enable/Disable 0: Internal Timer Interrupt gated to ***IP7*** 1: External **INT5*** gated to ***IP7***	25 1	On-chip secondary cache control. 0: Disable 1: Enable
12 1	Enable the external tertiary cache 0: Disable 1: Enable	26 0	Enable two outstanding reads with out-of-order return 0: Disable 1: Enable

NOTE THAT THE RM7000C XYLINX PROM BINARY STRING IS LITTLE ENDIAN: 10000000 01010101 00000001 00000010
*CPU is fed these boot mode bits as bytes in little endian mode. 7 -> 0 15 -> 8 23 -> 16 32 -> 24

These values ABOVE ARE in the order in which they are given in the table itself LSB -> MSB
Byte flipped from the above yields: 0 -> 7 8 -> 15 16 -> 23 24 -> 31
600MHz RM7000C mode bits: 00000001 10101010 10000000 01000000

NOTE: IN ORDER TO OBTAIN BOOT-MODE VALUES WHICH MAKE SENSE FOR THE 600MHZ CPU BYTE FLIPPING IS REQUIRED

Mode bit	Description	Mode bit	Description
[14:13] **10**	Output driver strength - 100% = fastest 00: 67% strength 01: 50% strength 10: 100% strength 11: 83% strength	[255:27] **0**	Reserved: Must be zero
15 **0**	External Tertiary cache RAM type: 0: Dual-cycle deselect (DCD) 1: Single-cycle deselect (SCD)		

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