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Section 3 Indy System Boards

The Indy CPU is mounted on an easily changed CPU module daughtercard that can be swapped without changing the rest of the system board. This provides an easy upgrade path for newer and faster CPUs.

Three CPU modules are currently available:

- R4600PC

- R4600SC
- R4400SC

The 100 MHz R4600PC module is based on the MIPS R4600 CPU; the 133 MHz R4600SC module is based on the MIPS R4600 CPU; and the 150 MHz R4400SC is based on the MIPS R4400 CPU. All three CPU modules include data and instruction caches (16 KB each) and a high-performance FPU. In addition, the R4600SC and R4400SC provide a secondary unified cache of 512 KByte and 1 MByte respectively.

The Indy system board offers many exciting standard features:

- a Fast SCSI-2 disk controller
- both AUI and 10Base-T Ethernet
- an enhanced audio architecture
- a video subsystem supporting SGI Digital Video input and NTSC/PAL composite and S-Video inputs
- ISDN connectivity
- 72-bit wide (64 bits plus parity) CPU and I/O buses for enhanced performance

The system board's main memory capacity is a full 256 MByte of DRAM, implemented with standard 36-bit-wide DRAM SIMMs.

Indy contains six major subsystems: the CPU, memory, graphics, I/O, video, and GIO expansion subsystems. The electronics are partitioned into the system board, the graphics board, and the CPU module daughtercard as illustrated in [Figure 2](#).

Note: Figure 2 includes the Indy Graphics subsystem. For information on XZ Graphics, see [Section 5](#).

FIGURE 2 Indy system electronics partitioned into subsystems and boards.
Shaded components represent custom ASICs from Silicon Graphics.

The bottom system board contains the memory, I/O and video subsystem. The CPU module is attached to the system board with two 80-pin connectors. The memory SIMMs are connected to the system board with eight 72-pin SIMM sockets.

The graphics board contains the graphics and GIO32-bis expansion subsystems. It is attached to the system board with two 96-pin connectors. Two GIO options boards can be connected to the GIO32-bis expansion subsystem through four 96-pin connectors.

The CPU subsystem contains the processor, EEPROM, oscillator and cache RAM. It is connected to the Memory Subsystem by a 64-bit (plus parity) multiplexed address and data CPU Bus.

The memory subsystem contains memory control, data bus routing and 8 SIMM sockets for main memory. A 64-bit (plus parity) multiplex address and data GIO64 bus connects the memory subsystem to I/O, graphics, video, and the GIO expansion subsystems.

The I/O subsystem contains a central I/O controller to collect data from relatively slow

peripherals and transfer it into main memory at high speeds. This controller includes support for boot PROMs, processor interrupts, a real-time clock, serial ports, a parallel port, ISDN, and audio. These peripherals are interfaced to the I/O controller by a 16-bit Peripheral Bus called the P-Bus.

The controller also supports a SCSI-2 controller and an Ethernet controller which are connected directly for increased bandwidth.

The video subsystem contains a video decoder chip set to convert analog NTSC/PAL video into digital pixels. The output of the decoder is connected to a video controller ASIC which formats and sizes the pixels and transfers them into system memory.

The Indy Graphics subsystem consists of the raster engine, the frame buffer, video timing controller, and the DACs (digital to analog converters). It is connected to the GIO64 bus. (For information on XZ Graphics see [Section 5](#).)

The GIO expansion subsystem is connected to 32-bits of the GIO64 bus. It also has a direct connection to the video backend section of the graphics subsystem.

3.1 Custom ASICs

Silicon Graphics developed several custom ASICs to aid communication between the system and the buses:

- The MC1 ASIC performs many functions, such as the GIO64 bus arbiter, which provides an interface between the CPU and the GIO64 bus. It is also the memory controller, allowing direct memory access (DMA) by devices other than the CPU.
- DMUX1 ASICs are data path chips, controlled by the MC1 chip, that isolate the CPU bus from the GIO64 bus. They also perform the memory interleaving functions.
- The HPC3 ASIC provides an interface to peripheral I/O, the audio system, and other devices on the P-Bus, connecting them to the GIO64 bus.
- The IOC1 ASIC provides interrupt control, two general purpose serial ports, a parallel port, and a keyboard/mouse controller.
- The REX3, located on the Indy Graphics board, connects the graphics subsystem to the GIO64 bus and renders pixels into the framebuffer.
- The HAL2 ASIC provides the data path and control logic to interface the HPC3 P-Bus and audio.
- The VINO ASIC processes digital video pixels and DMAs them into system memory in both RGB and YUV formats.

3.2 CPU Subsystem

The CPU subsystem is designed to accommodate future members of the R4000 family of CPUs. The subsystem is mounted on an easily changed CPU module daughtercard that can be swapped without changing the rest of the system board. The module consists of the CPU, an oscillator to set the processor speed, and a serial EEPROM. Some modules also contain secondary cache memory.

3.2.1 Pipelining

The entire R4000 family of CPUs supports both the MIPS I instruction set and the MIPS III instruction set. Data pathways in MIPS III are 64 bits wide, giving the system the ability to load and store full floating point double words in a single machine cycle. The MIPS III instruction set also contains synchronization and advanced cache control primitives.

The R4400 CPU uses superpipelining to achieve the fast internal speed. In normal pipelining, the CPU breaks each instruction into separate one-cycle steps (usually fetch, read, execute, memory, and write back), and then executes instructions at one-cycle intervals. Pipelining allows instructions to overlap, providing close to one instruction per cycle instead of one instruction every five cycles.

At the fast R4400 CPU clock rate, some instruction steps such as cache reads and writes can't execute in a single pipelined cycle. Superpipelining executes each of these critically slow steps in a single cycle to provide higher throughput. To do so, it first breaks instruction steps into substeps. The substeps are then pipelined in a process separate from standard pipelining, which executes the full step in a single cycle. R4400 superpipelining is optimized so that it requires little control logic and instruction structure, unlike SuperScalar implementations.

Instead of Superpipelining, the R4600 CPU achieves its speed with a simple five-stage pipeline offering minimal penalties (one cycle each for branch or load use). The R4600 does virtual-to-physical translation in parallel with cache access allowing it to support a large TLB for address translation.

3.3 CPU Bus

The CPU Subsystem is connected to the Memory Subsystem by a 64-bit wide (plus parity) data and address CPU Bus. This bus consists of the R4600/R4400 bus and control signals from the memory subsystem. It runs at 50 Mhz as set by the CPU oscillator and can transfer data at 267 MBytes per second to and from the memory subsystem.

3.4 Memory Subsystem

The memory subsystem uses two types of custom chips, the MC1 ASIC and the DMUX1 ASIC, to give the CPU access to main memory and the GIO64 bus and to isolate the CPU bus from the GIO64 bus.

The MC1 ASIC, the Memory Controller (shown in Figure 3, is a custom Silicon Graphics chip connected to the CPU module by the CPU bus. It's also connected to the GIO64 bus (the I/O bus), and has address and control lines connected to main memory. It performs many functions:

- It controls the flow of data between main memory and the CPU.
- It serves as a DMA (Direct Memory Access) controller for all memory requests from the graphics system or any other devices on the GIO64 bus.
- It acts as a system arbiter for the GIO64 bus.
- It provides single-word accesses for the CPU to GIO64 bus devices and to the

graphics system.

- It passes on interrupts from the IOC1 ASIC to the CPU.
- It initializes the CPU on powerup, executes CPU requests, refreshes memory, and checks data parity in memory.

FIGURE 3 A block diagram of the MC1 ASIC. The MC1 runs the system bus, handles memory access for CPU and GIO64 devices, works as a DMA controller, and fulfills other miscellaneous functions.

The DMUX1 ASICs are a two-chip slice of a data crossbar between the CPU, main memory, and the GIO64 bus. The two DMUX1 chips are, together, a data path with control signals generated by the MC1. They isolate the CPU bus from the memory system and the GIO64 bus. They also contain synchronization FIFOs to perform flow control between the various subsystems and they interleave main memory to increase peak memory bandwidth.

3.4.1 Main Memory

Main memory, which is controlled by the MC1 and DMUX1 ASICs, provides system access to large amounts of DRAM. Memory consists of standard off-the-shelf 36-bit wide DRAM SIMMs (which must have 80 ns RAS access time and fast page-mode capability). To support the increased bandwidth of the R4600/R4400 CPU, the DMUX1 chips interleave the SIMMs to create a 72-bit wide two-way interleaved memory system. See Figure 4.

FIGURE 4 Memory on the Indy system board interleaves SIMM strips in banks of four, and connects them to the CPU and the GIO64 bus with DMUX1 and MC1 chips.

Main memory can be configured to be as little as 16 megabytes or as much as 256 megabytes. The system board has 8 SIMM sockets, arranged in two banks of four. Each bank must use SIMMs of the same size, but SIMM sizes can differ between banks to allow different memory configurations.

3.5 GIO64 Bus

The GIO64 bus, the main system bus, provides a 64-bit wide (plus parity) data path and is designed for very high speed data transfer. It connects the Indy main systems: the CPU, memory, graphics, I/O, video and GIO expansion slots. The GIO64 is a synchronous, multiplexed

address/data burst mode bus that runs at 33 MHz and is clocked independently of the CPU. The GIO64 bus can transfer data between main memory and any device on the bus at up to 267 MBytes per second.

3.6 The I/O Subsystem

The I/O system ties together a variety of I/O ports and the chips that drive them, a system clock, and the system PROM for booting up.

The HPC3 ASIC (High Performance Peripheral Controller) is the heart of the I/O subsystem. It is a custom Silicon Graphics chip that collects data from relatively slow peripherals, buffers it in FIFOs and then transfers it into main memory using high speed DMA transfers over the GIO64 bus. It also transfers data from main memory to peripheral devices in the same manner.

The HPC3 has direct interfaces to the GIO64 bus, to a SCSI-2 port, to an Ethernet port and to the 16-bit P-Bus (Peripheral Bus). SCSI and Ethernet ports are connected directly for increased bandwidth. The P-Bus is a 20-bit address, 16-bit data bus used by the HPC3 for additional peripheral support. It connects the boot PROM, a real-time clock, the audio system through the HAL2 ASIC, the ISDN interface, and the IOC1 ASIC. The IOC1 integrates an interrupt handler, two general purpose serial ports, a parallel port, and a keyboard/mouse controller with two bit-serial interfaces for PS/2 style keyboard and mouse ports. There is a 384 byte memory buffer that is shared by all of the P-Bus devices to buffer DMA transfers to and from memory.

3.6.1 Ethernet Port

The Ethernet interface consists of both an AUI and a 10BASE-T Ethernet port supported by a controller that is connected directly to the HPC3 ASIC. The interface automatically selects between the AUI and 10Base-T ports. The HPC3 supplies the logic required to retransmit packets when collisions occur and to manage the interface's 64-byte FIFO buffer. When the HPC3 receives a packet, it interrupts the CPU after it writes the packet into memory. When transmitting, it interrupts the CPU when a packet is successfully sent or when 16 transmission attempts have all failed.

3.6.2 SCSI-2 Port

The Fast SCSI-2 interface consists of one channel shared between internal and external devices. The channel supports two internal SCSI devices and up to five external SCSI devices through a high-density SCSI port on the rear of the system unit.

The Fast SCSI-2 channel is supported by a SCSI controller connected directly to the HPC3 ASIC. The HPC3 uses a FIFO buffer to enable burst use of the GIO64 bus.

3.6.3 Parallel Port

The parallel interface consists of a bidirectional Centronics parallel port controlled by the IOC1 ASIC that connects to the P-Bus and provides a FIFO buffer used to transfer data between main memory and the parallel port at up to 1.0 MByte/sec.

3.6.4 Serial Port

The serial interface consists of two serial ports, controlled by the IOC1 ASIC that connects to the P-Bus. The serial ports are software programmable for RS-422 (differential) and RS-232 standards and support a transfer rate of up to 38.4 Kbits per second. The RS-422

standard allows the use of common Macintosh peripherals such as laser printers and scanners. Support for MIDI timing is also provided.

3.6.5 Keyboard and Mouse Ports

The keyboard and mouse ports are controlled by the IOC1 ASIC and provide a standard PS/2 interface.

3.6.6 ISDN Port

Indy supports a single ISDN basic rate interface integrated onto the system board. Access to the ISDN is provided at the "S" access point. The design provides a single hardware implementation that is certifiable throughout the world.

The ISDN basic rate interface on Indy supports the Point-to-Point-Protocol (PPP). PPP enables TCP/IP networking across ISDN B-channels, providing the full 64 Kbit per second band width of each B-channel.

The Application Software Interface (ASI) being developed by the National ISDN User's Forum is expected to become a standard in the USA. It will be available on Indy for developing applications such as telephone management applications.

ISDN features include:

- single "S" RJ45 access connector
- hardware HDLC framing on both B-channels for data communications and networking applications
- 3 DMA channels (one channel to transmit and one each for the receive direction on each B-channel)
- separate 64 byte transmit and receive FIFOs on each B-channel and on the D-channel

A block diagram of the Indy ISDN architecture is shown in Figure 5.

FIGURE 5 ISDN interface architecture.

The interface is based on the S interface chip and the HDLC controller chip. The S interface chip provides the interface to the 4-wire S interface, HDLC formatting on the D-channel, two FIFOs for the D-channel transmit and receive data, and host access to the D-channel data. The HDLC controller chip provides the DMA interface to the B-channels, HDLC formatting on the B-channels, and four FIFOs for the B-channel transmit and receive data. The isolation transformers provide the coupling and high voltage isolation between the S interface and the Indy system.

The S interface chip and the HDLC controller chip are both connected to the P-Bus in the Indy system. Both chips contain registers that may be accessed by the host CPU. The

HDLC controller chip is connected to three DMA channels that are contained in the HPC3 ASIC.

3.6.7 Audio

The system board provides the ability to record, process, synthesize and play professional quality audio. Indy audio retains binary compatibility for application programs through the use of Silicon Graphics Audio Library (AL). Figure 6 illustrates the audio architecture.

FIGURE 6 Indy audio architecture.

Indy audio provides the following features:

- built-in speaker
- volume controls on the front of the Indy system unit
- stereo line level analog audio input and output
- stereo headphone output
- AES/EBU digital audio input and output
- sampling rates of 48 kHz, 44.1 kHz, 32 kHz, 16 kHz, 8 kHz, and more
- microphone input with DC power
- simultaneous input and output
- independent input and output rates
- output rate can be synchronized to the digital input rate
- professional quality analog signal processing
- Silicon Graphics Audio Library (AL) API
- low latency operation for highly interactive applications
- microphone input supports stereo microphones
- time-stamped samples
 - utime format time stamps on every sample frame
 - time stamps are synchronized with CPU time base
 - additional bits give resolution to 0.1 microsecond
- non-audio bit tagging on audio samples
 - left and right analog clip indicator bits
 - P, C, U, and V bits for digital audio samples
- four-channel mode supports four analog channel input and four analog channel output, simultaneously, at full speed
- analog audio input and serial digital audio input can occur simultaneously
- analog audio output and serial digital audio output may be independent
- analog audio input may be synchronized to digital audio input
- sampling time base is generated by Bresenham's algorithm, allowing near continuous choice of sample rates

HAL2 ASIC

The Indy audio system is built around a central controller chip, the HAL2 ASIC, two stereo audio CODEC chips, an AES transmitter chip, an AES receiver chip, a microphone input circuit, a headphone/speaker amplifier circuit, and a four-channel-mode output

switch. The HAL2 contains the data path and control logic to interface the HPC3 P-Bus and the audio devices on the module.

The HAL2 includes three independent clock generators---AES out, analog in, and analog out---that each can select from three different timebases. The clock generators use Bresenham's algorithm to scale the input clocks by rational fractions. The time-stamping clock is generated from the same timebase as the unix utime. Each audio device has its own DMA channel and clock generator with the channel allocation configurable in software. The audio devices attach with conventional 3-wire serial interfaces. In 4-channel mode, data from all four channels goes over the same DMA channel guaranteeing synchronization.

Codecs

Indy audio uses a pair of stereo audio Codecs. These chips are highly integrated monolithic CMOS mixed-signal devices that make use of the latest signal conversion technology. Both the analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are 64x-oversampling delta-sigma 16-bit converters. They also contain on-chip reconstruction and antialiasing filters, programmable input gain, and programmable input source switching. The filters' responses track the sampling rate, a significant advantage over the older fixed-response low-pass analog filter designs.

In the normal mode of operation, the Codec A DAC is used for analog output and the Codec B ADC is used for analog input. The Codecs can use independent sample-rate clock generators from the HAL2, so that the analog input sample rate and the analog output sample rate may be selected independently. The analog input (to Codec B) is selectable from either the line or microphone inputs under software control. The analog output signal (from Codec A) is routed both to line-out and to the stereo headphone/internal loudspeaker circuit. The user gets true line-level signal and a volume-adjusted headphone/loudspeaker output.

Indy audio provides an enhanced mode of operation that extends the number of simultaneously active analog input channels from 2 to 4 and the number of simultaneously active analog output channels from 2 to 4.

In 4-channel mode, both Codecs are synchronized to the same sample rate and the Codecs are used simultaneously for input (ADC) and output (DAC). Codec A's input (ADC) comes from the microphone input, Codec B's input (ADC) from the line input. Codec A's output continues to be routed to the line output, but Codec B's output is routed at line-levels to the headphone jack.

Serial Digital Audio Transmitter

Indy has an industry-standard, transformer-coupled, serial digital audio output that supports up to 24-bit stereo samples at all available sample clock rates. The audio and non-audio bits may be coded to support both professional and consumer standards (AES3, IEC958).

Serial Digital Audio Receiver

Indy has an industry-standard, transformer, coupled, serial digital audio input that supports up to 24-bit stereo samples at up to a 50 kHz sample rate. The sample rate clock recovered from this input may be used to generate synchronized sample clocks for the Codecs and serial digital audio transmitter. All of the bits received in the serial digital channel including U, C, V, and P are input to the computer. Both professional and consumer coding formats are supported by AES3, IEC958.

Microphone

Indy comes standard with a high-quality, electret condenser monaural lapel microphone. The microphone is omnidirectional and has both a wide-frequency response and a large dynamic range.

The Indy microphone input circuit provides DC power for active circuitry in microphones that require it, while retaining compatibility with other types of microphones. Powered microphones, such as the one supplied with Indy, use this DC power to drive a large low-impedance signal back to the audio circuitry, avoiding the problems commonly associated with low-level microphone signals and electrically noisy computer environments.

The microphone input circuit accepts both monaural and stereo microphones. In addition to the input source switching and software-controlled gain functions available in the Codecs, the DC power feature and a hardware 20 dB gain stage may be enabled and disabled via software control.

Internal Speaker

The internal speaker in Indy audio outputs the sum of the left and right line-out channels. The speaker is shielded to protect the graphics and video monitors from the speaker's magnetic field. Speaker volume is software controlled.

Headphone Output

The Indy audio system provides a stereo headphone output connection, suitable for connecting standard headphones without need for external amplifiers. The headphone volume for each channel is software controlled. When a headphone is plugged into the connector, the internal speaker is automatically disconnected.

3.7 The Video Subsystem

The video subsystem provides a low-cost way to capture and use video and video mail as a computer data type in presentations, in user-to-user communications (like video conferencing) and in documentation and training. The subsystem displays video live in a window.

Indy comes standard with the IndyCam(tm), a digital color video camera. There are three video input ports to support different video formats:

- NTSC/PAL composite analog video
- NTSC/PAL S-Video analog video
- SGI Digital Video

A block diagram of the video subsystem is shown in Figure 7. The video subsystem inputs video, digitizes the analog video, processes the digital pixels as requested, and then puts the pixels on the GIO64 bus. The subsystem provides pixel formatting and DMA hardware to assist software implemented video compression and decompression.

FIGURE 7 Video subsystem architecture.

The video subsystem is built around the VINO ASIC shown in Figure 8. There are two DMA Channels (A and B) within the VINO ASIC. Either channel can be assigned to the SGI Digital Video input bus or the Phillips (analog input) bus. Both channels can be used simultaneously; however, only one analog format can be used at any one time.

For example, the following channel combinations are possible:

- both channels can be connected to the digital video input
- one channel can be connected to the digital video input and one to either Phillips analog video input
- both channels can be connected to the Phillips composite video input
- both channels can be connected to the Phillips S-Video input

3.7.1 Video Processing

Digital video from the SGI Digital Video port is sent directly to the VINO ASIC illustrated in Figure 8. Analog video from either the composite or S-Video port is first input to a digital decoder chip set for conversion to digital pixels which are then sent to the VINO ASIC. The VINO ASIC can then resize the digital pixels and color space convert them before it DMA's them into system memory in both RGB and YUV formats. The clipping, decimation/filtering, color space conversion, and dithering processes are optional, allowing NTSC/PAL video with full spatial, temporal, and color information.

Four pixel formats are supported when transferring pixels from the VINO ASIC into system DRAM:

- 32-bit RGBalpha
- 16-bit YUV (4:2:2)
- 8-bit RGB
- 8-bit monochrome

From system DRAM, the RGB pixels are transferred to the graphics subsystem to be displayed. The YUV pixels can be compressed using software algorithms and saved on the system disk, or they can be transferred over a network to another Indy system.

FIGURE 8 VINO ASIC block diagram.

3.7.2 IndyCam

The IndyCam is a highly integrated digital color video camera bundled with each Indy system. It provides a real-time digital data stream directly to the VINO ASIC for subsequent processing and DMA. IndyCam generates color image data at 60 Hz in an interlaced field and provides a resolution of 640 x 480 pixels. Figure 9 illustrates the IndyCam in a block diagram.

Power and serial control are passed to the IndyCam through the SGI Digital Video connection on the Indy back panel. The serial control allows you to manipulate shutter speed, color balance, gain, and automatic gain.

The SGI Digital Video standard is similar to the CCIR-601 digital video standard while providing more flexibility. Pixels per line and lines per scan are programmable in the VINO ASIC allowing the integration of non-standard imagery with the Indy system. In addition, voltage levels are TTL in the SGI digital video signal versus ECL in the CCIR-601 signal.

FIGURE 9 IndyCam block diagram.

