Advance

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Bt445

150 MHz Monolithic CMOS Triple 256 x 8 RAMDAC™

Distinguishing Features

- PLL Pixel Clock Generation (M/N)
- Up to 64-Bit Input Pixel Port Width
- 150, 135, and 110 MHz Operation
- High-Resolution True-Color Support
- 1:1 to 64:1 Multiplexed Pixel Port
- Bt458 Software Compatible
- Programmable Pixel Format
- Three 256 x 8 Color Palette RAMs
- 16 x 24 Overlay Palette
- 4 x 24 Cursor Palette
- Digital Pixel Output Port
- 0 or 7.5 IRE Blanking
- VRAM Shift Clock Generation
- System Clock Generation
- JTAG Support
- 160-pin PQFP Package

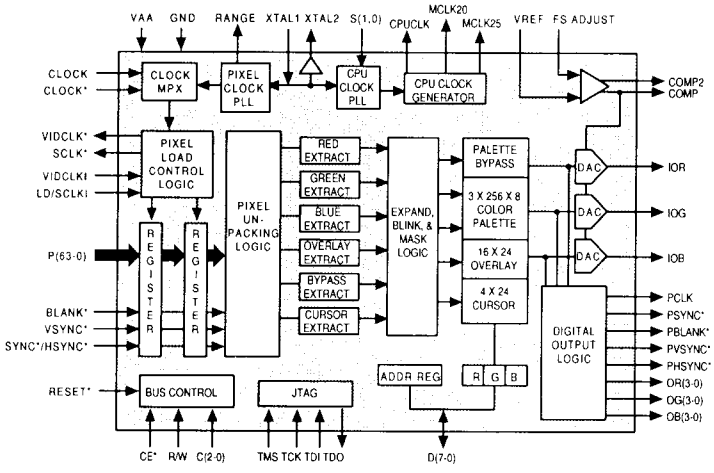
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Color Flat Panel Displays

Related Products

- Bt431
- Bt458
- Bt858

Functional Block Diagram



Product Description

The Bt445 is designed specifically for high-performance, high-resolution color graphics applications. The wide input pixel port and internal multiplexing modes enable TTL-compatible interfacing to the frame buffer, while maintaining PLL-generated 135 MHz, or externally provided 150 MHz video data rates required for high refresh rate, high-resolution color graphics.

The Bt445 supports PLL pixel clock generation, supporting a variety of frequencies using an M/N divisor scheme. This decreases system cost due to the elimination of multiple crystal oscillators that are used to support a variety of monitor and refresh rates. In addition, the Bt445 provides the serial VRAM clock, video clock, and various multi-purpose system clocks.

Using a patented pixel port architecture, Flexport™, the input pixel port can be configured in an almost unlimited variety of pixel depths, multiplex modes, and input port widths. For example, these modes include 1-, 2-, 4-, 8-, 12-, 16-, and 24-bit/pixel pseudo color and true color with overlay and cursor palette support. The Bt445 runs 24-bit true color, with cursor, overlay, and palette bypass support, at pixel rates for 1280 x 1024 monitors. The Bt445 is also Bt458 software compatible.

Other features include programmable setup and digital pixel outputs, as required for active matrix TFT support or NTSC encoding.

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Circuit Description

Introduction

The Bt445 is a flexible 150-MHz RAMDAC, which provides multiple multiplex operating modes with multiple plane depth resolutions, while still maintaining Bt458 register compatibility.

Two phase lock loops are provided to eliminate high-speed signals on the PCB and expensive ECL crystal oscillators. One is programmable ((M/N)/L), where M is 6 bits, N is 4 bits, and L can be 1, 2, 4, or 8) and is used to generate the pixel clock frequency. The second PLL operates from the same crystal or oscillator input as the pixel PLL, and is not programmable. It may be used to provide additional clock outputs that may be used for the CPU system clocks, and/or SCSI or Ethernet clocks, for example.

The Bt445's input pixel port can be software-configured to be any width from 1–64 pins. This allows maximum versatility for frame buffer configuration. For example, the Bt445 can support a frame buffer architecture having a 6:1 multiplexed 8-bit pseudo-color frame buffer (48 signals) with 2-bit overlay (12 signals). The input port width in this case may be set to 60 pins. A pixel display order can be selected to start from the lower-numbered bits of the input pixel port (LSB unpacking) or from the higher-numbered bits (i.e., the pixel port width, MSB unpacking).

The Bt445 also provides fully programmable multiplex rates (1:1 to 64:1, any integer value) and fully programmable pixel widths (1 to 32 bits per pixel, any integer value). The only restrictions are that the pixel port start position, multiplex rate, and pixel width be consistent. This means that the number of bits per pixel multiplied by the multiplex rate must be less than or equal to the number of input port bits configured. Also, when configured for 1:1 multiplexed, the maximum pixel rate is limited by the input pixel port rate, as indicated in the AC Characteristics section.

After pixel serialization has occurred, the Bt445 allows full configurability for source and width selection of the red, green, blue, overlay, cursor, and palette bypass fields of the source pixel. For example, in a 16-bit wide pixel, the red field may come from bits 4–0, green may come from bits 9–5, blue may come from bits 14–10, and palette bypass control may come from bit 15 of the pixel.

Pseudo-color modes are supported by sourcing the red, green, and blue fields from the same bits in the source pixel. In fact, any fields of an input pixel may appear in any order or be coincident or overlapped with other fields.

The color palette bypass bit controls the selection between color palette usage or bypass. Users can use the lookup table for gamma correction or they can bypass the LUT on a pixel-by-pixel basis. This allows users to customize features with ASICs, while providing capabilities for cost-efficient high-resolution 1280 x 1024 true-color graphics. Color palette bypass is available in all pixel modes, allowing numerous monochrome/gray-scale options on the Bt445.

The Bt445 also provides a digital pixel output port from the DAC inputs to support driving an active matrix TFT LCD or an NTSC encoder such as the Bt858. The Bt445 provides a clock, and the red, green, and blue pixel data prior to the decoder of the DACs. In addition, the pipelined sync and blank outputs are provided so that users can synchronize their timing to valid pixel data. Two modes of operation are provided: 4-4-4 true color where the high-order nibble of red, green, and blue are provided, and an 8-8-8 true-color mode where all bits of red, green, and blue are provided at a reduced pixel rate. When using the digital output port (i.e., output bits OR3–OR0, OG3–OG0, or OB3–OB0), the DAC output quality is not guaranteed.

For battery-powered applications, various power-down modes are available. In one mode, the RAM and DACs are turned off. The RAM retains data and may be accessed for read or write operations by the MPU. Another mode powers down the pixel clock, RAM, and DACs. A video RAM shift clock (SCLK*) is provided by the Bt445, changing the cycle frequency in correspondence with the multiplex factor. This simplifies timing requirements to develop external logic for VRAM timing generation. In addition, the Bt445 provides another output clock (VIDCLK*) which should be used for the generation of the CRT timing signals.

Circuit Description *(continued)*

MPU Interface

As illustrated in the functional block diagram, the Bt445 supports a standard MPU bus interface, allowing the MPU to access the internal control registers and color palettes. The dual-port color palette RAM, overlay palette, and cursor color registers allow color updating without contention with the display refresh process.

Table 1 illustrates how the C(2–0) control inputs work in conjunction with the internal address register to specify which control register, color palette RAM entry, overlay register, or cursor color register will be accessed by the MPU.

The reset pin presets the internal registers, defaulting all internal registers to be compatible with the 4:1 multiplex configuration of the Bt458. Features such as alternate pixel depth modes and multiplex factors are available through the use of the C(2) control pin, which provides access to the extra features.

The 8-bit address register (ADDR(7–0)) is used to address the internal color and control registers, eliminating the requirement for external address multiplexers. ADDR(0) corresponds to D(0) and is the least significant bit.

Reading/Writing Color Data

To write color data the MPU loads the address register with the address of the color palette RAM location, overlay palette, or cursor color register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C(2–0) to select the color register. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C(2–0) to select either the color palette RAM, overlay palette, or cursor color registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR(7–0)) are accessible to the MPU.

Additional Information

Although the color and overlay palette RAMs and cursor color registers are dual ported, if the pixel data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers can also be accessed through the address register in conjunction with the C(2–0) inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

To prevent pixels from being disturbed during writes to the control registers, the MPU data must be valid during the entire chip enable time, or the accesses should be limited to blanking time. The setup time shown in the AC Characteristics section are the minimum required to internally capture the data.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU. This is not recommended, as this may cause problems in Bt445 code-compatible products.

Circuit Description *(continued)*

C(2-0)			ADDR(7-0)	Reset Value [Hex]	Addressed by MPU
0	0	0	$xx		Address Register
0	0	1	$00–$FF		Primary Color Palette RAM*
0	1	0	$00	3A	ID Register ($3A)
			$01	A0	Revision Register ($A0)
			$02		Reserved
			$03		Reserved
			$04	FF	Read Enable Register
			$05	0	Blink Enable Register
			$06	43	Command Register 0
			$07	0	Test Register 0
			$08–$FF		Reserved
0	1	1	$00–$0F		Overlay Color Palette RAM (Note 1)
			$10–$FF		Reserved
1	0	0	$xx		Reserved
1	0	1	$00	07	Red MSB Position
			$01	08	Red Width Control
			$02	FF	Red Display Enable Control
			$03	0	Red Register Blink Enable
			$04–$07		Reserved ($00)
			$08	07	Green MSB Position
			$09	08	Green Width Control
			$0A	FF	Green Display Enable Control
			$0B	0	Green Blink Enable Register
			$0C–$0F		Reserved ($00)
			$10	07	Blue MSB Position
			$11	08	Blue Width Control
			$12	FF	Blue Display Enable Control
			$13	0	Blue Blink Enable Register
			$14–$17		Reserved ($00)
			$18	09	Overlay MSB Position
			$19	02	Overlay Width Control
			$1A	03	Overlay Display Enable Control
			$1B	0	Overlay Blink Enable Register
			$1C–1F		Reserved ($00)
			$20	0	Cursor MSB Position
			$21	02	Cursor Width Control
			$22	03	Cursor Display Enable Control
			$23	0	Cursor Blink Register
			$24–$FF		Reserved ($00)

Table 1. Address Register (ADDR) Operation.

Circuit Description *(continued)*

C(2–0)			ADDR (7–0)	Reset Value [Hex]	Addressed by MPU
1	1	0	$00	0X	Test Register 1
			$01	40	Command Register 1
			$02	0	Digital Output Control Register
			$03	03	VIDCLK* Cycle Control Register
			$04		Reserved
			$05	19	Pixel PLL Rate Register 0
			$06	04	Pixel PLL Rate Register 1
			$07	XX	PLL Control Register
			$08	04	Pixel Load Control Register
			$09	28	Pixel Port Start Position Register
			$0A	08	Pixel Format Control Register
			$0B	03	MPX Rate Register
			$0C	XX	Signature Analysis Registers (Note 1)
			$0D	0A	Pixel Depth Control Register
			$0E	0	Palette Bypass Position
			$0F	01	Palette Bypass Width Control
			$10–$FF		Reserved ($00)
1	1	1	$00		Cursor Color 0 (Note 1)
			$01		Cursor Color 1 (Note 1)
			$02		Cursor Color 2 (Note 1)
			$03		Cursor Color 3 (Note 1)
			$04–$FF		Reserved

Note 1: Requires modulo 3 loading/reading.

Table 1. (continued). Address Register (ADDR) Operation.

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Circuit Description *(continued)*

Clock Generation

The Bt445 has two phase lock loops for generating the pixel clock and three system clocks. (See the Functional Block Diagram and Figure 1). The pixel clock is fully programmable, able to generate over 500 unique pixel clock frequencies using a single crystal.

The advanced phase lock loops (PLLs) contain an internal loop filter to provide maximum noise immunity and reduce jitter. Except for the reference crystal or oscillator, no external components or adjustments are necessary.

The pixel clock generator uses an M over (L x N) scheme to provide precise frequencies. The M, N, and L values can be programmed through the command registers with a variety of values, which generally provide frequency granularity that averages less than 1 MHz. M is a binary 6-bit value, N is a binary 4-bit value, and L is selectable to be 1, 2, 4, or 8. Serial clock and video clocks are generated from the derived pixel clock.

A second PLL generates a number of various clocks (MCLK20, MCLK25, CPUCLK), which may be used for the CPU clock and other system clocks. Using a 20 MHz crystal, a constant 20 MHz and 25 MHz clock is available for Ethernet and SCSI clock generation, while the CPU clock output is selectable between 25, 33, 40, or 50 MHz. The reference crystal used must be an AT cut, with series configuration, and operated in the fundamental mode. An oscillator reference can also be used by capacitively coupling the oscillator's output to the XTAL1 input, as shown in Figure 2. For this configuration, leave the XTAL2 pin disconnected as shown.

Both PLLs can be disabled separately to provide maximum flexibility in configuring the Bt445 to match the system requirements. In order to minimize noise, all unused outputs should be disabled via the command registers. Additionally, in order to provide minimal noise effects to the RAMDAC, all of the clock generated outputs are low drive and must be redriven by a buffer before distribution.

With the assertion of RESET*, the video clock defaults into a mode whereby a one-fourth pixel rate video clock is automatically generated. This rate is consistent with the LD rate needed to use a Bt458 in 4:1 multiplex mode. The PLLs are also initiated with RESET* to generate the system clocks.

As an alternative to using the PLL for pixel clock generation, the Bt445 is also designed to accept differential clock signals (CLOCK and CLOCK* in Figure 2). These clock inputs can be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close to the driving source as possible. A 150-Ω chip resistor near the RAMDAC pins is also needed to ensure proper termination. (See Figure 3).

Circuit Description *(continued)*

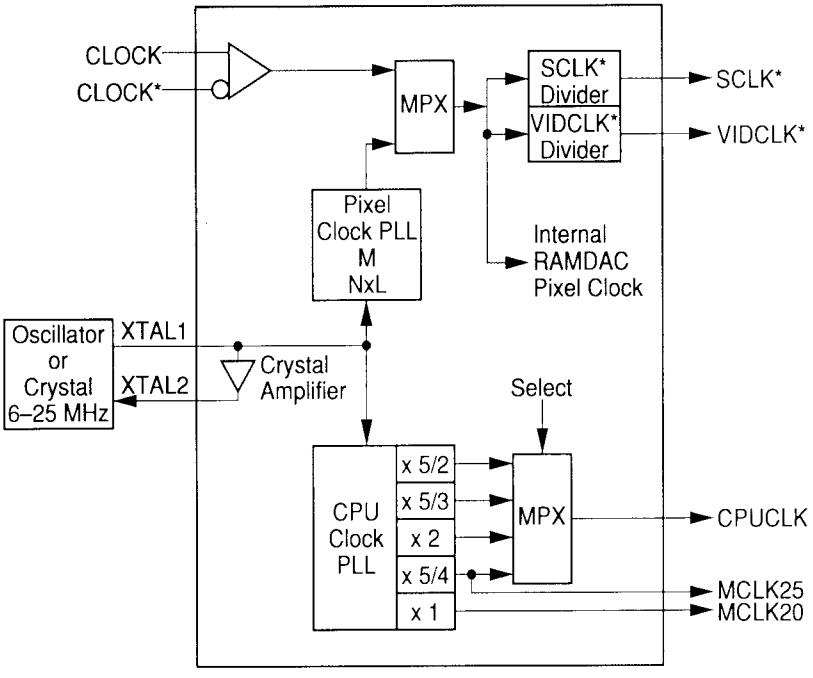

Figure 1. PLL Clock Generation Block Diagram.

Circuit Description *(continued)*

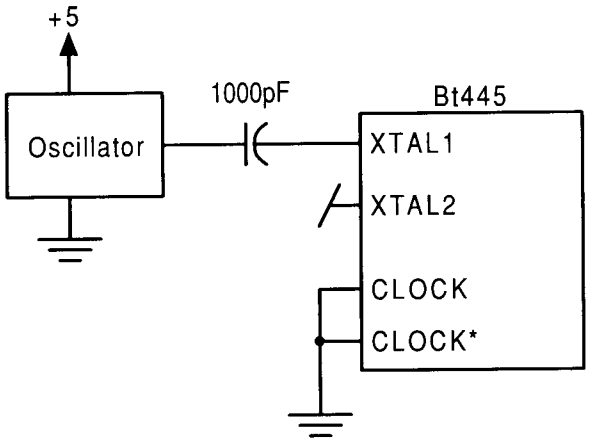

Figure 2. Oscillator Clock Interface.

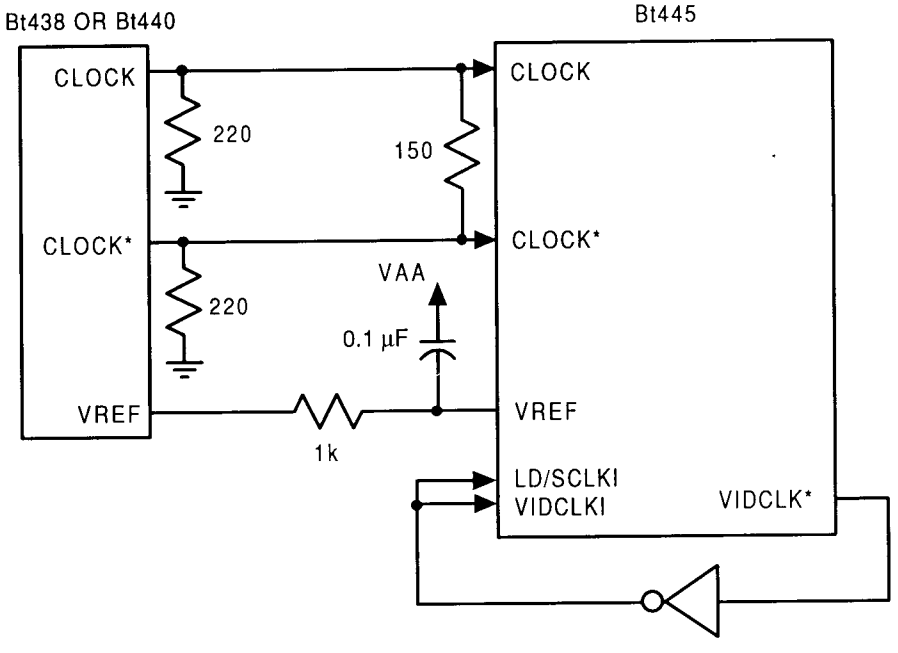

Figure 3. Differential ECL CLock Interface.

Circuit Description *(continued)*

Frame Buffer Clocking

Pixel data may be clocked into the Bt445 in one of two modes: with VIDCLK input and output signals, or with the SCLK input and output signals.

Pixel Loading Using SCLK

System designs that interface VRAM frame buffer serial data directly to the Bt445 can use the SCLK* and LD/SCLKI signal pairs to load pixel data. In this mode, the Bt445 facilitates the generation of the VRAM shift clock by providing VRAM serial shift clock, SCLK*. SCLK* should be used to clock the VRAM shift registers that provide pixel data to the Bt445. The ratio of SCLK* to the pixel clock equals the value set into the MPX rate register.

SCLK* is stopped (in a logical "1" state) during blanking to allow the system to reload the VRAM serial shift registers. System implementations using "midline" transfer may necessitate inserting a VRAM shift clock pulse during blanking time to load the shift register tap address. The system may insert this additional clock without incurring additional gate delays by using a NAND driver for generating SCLK to the VRAMs. The unused input on the NAND driver may be used to insert the additional SCLK to load the tap address. The SCLK* (active low time) pulse width is nominally two pixel clock cycles; as a result, architectures using less than 4:1 multiplexing will not normally use the SCLK*/SCLKI signals for pixel loading. Also refer to the AC timing specifications for the maximum rates at which the SCLK* may be operated.

The buffered version of SCLK*, referred to in this specification as SCLK, is returned to the Bt445 to be used to load the input pixel data. This allows for faster serial path operation, as the buffer delay does not add to the serial port delay in determining the minimum SCLK cycle time at which the system may operate (refer to Figures 4 and 5).

The VIDCLKI signal is still used to load the VSYNC*, HSYNC*, SYNC*, and BLANK* signals. The VIDCLK rate is independent of the pixel depth; the VIDCLK rate is selected by the VIDCLK rate select register.

Pixel Loading Using VIDCLK

System architectures that preclude using the SCLK signals for loading pixel data may instead use the VIDCLK* signal to load pixel data. In this mode of operation, the LD/SCLKI and VIDCLKI should be connected together.

In this mode, the VIDCLK rate select field should be written as the same value as the MPX Rate Register. The SCLK* output is disabled (high-z) when the Bt445 is configured in this mode.

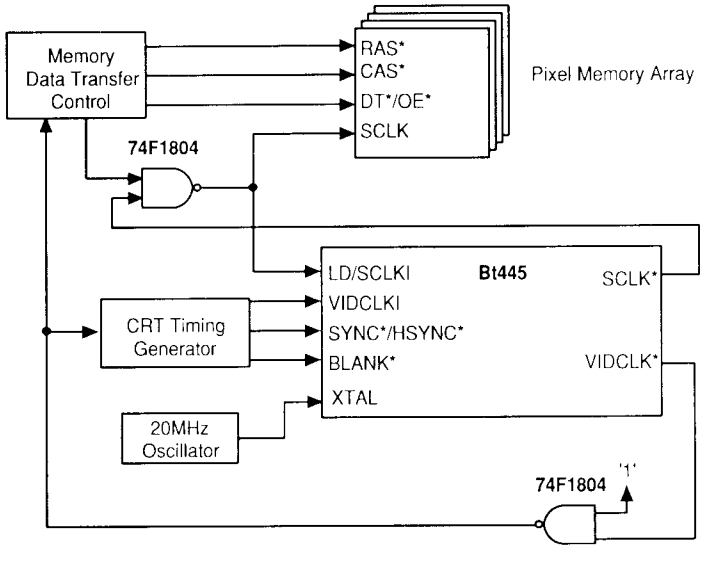

Figure 4. Frame Buffer Clocking Interface, Using SCLK.

Circuit Description *(continued)*

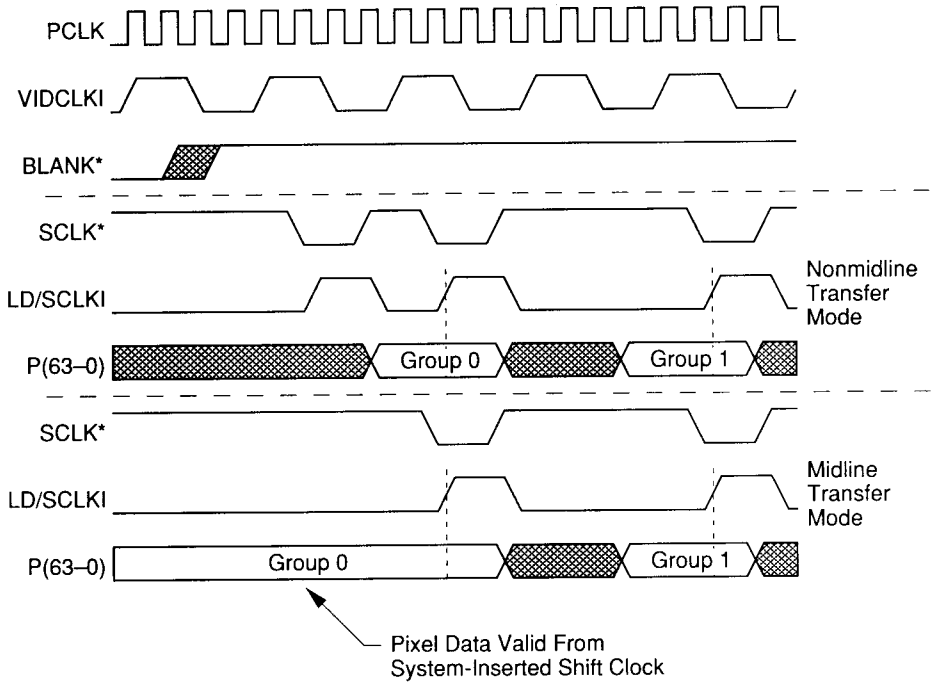

Figure 5. Frame Buffer Interface Timing Diagram Using SCLKI.

Circuit Description *(continued)*

VIDCLK Generation

At reset time, the Bt445 is configured to load pixels using VIDCLK. The multiplex rate is set to 4:1 (Bt458 compatible). When changing the VIDCLK rate, the VIDCLK* output is guaranteed not to glitch when changing from one rate to another. During the transition, the minimum low or high pulse width will be at least the low or high width of the faster of the old or new VIDCLK rate. For 1:1 and 2:1 VIDCLK* rates, the VIDCLK* output will have a 50/50 duty cycle; for 3:1 to 64:1 VIDCLK* rates, the VIDCLK* active (low) pulse width is 2 pixel clocks.

Video Generation

The VIDCLK* output is a free-running clock typically used for clocking the display timing generator. The period of VIDCLK* is independent of SCLK* and is controlled by the MPU by the VIDCLK* rate register. VIDCLK may be the pixel clock divided by any integer from 1–64. SYNC* and BLANK* information are registered with each rising edge of VIDCLKI and inserted into the pipelined pixel stream at the appropriate time.

When using SCLK* to clock pixels, SYNC* and BLANK* are registered by a different clock from the pixel data; therefore, they do not correspond to the pixel inputs that are present at the same time. The SYNC* and BLANK* inputs are used to provide the RAMDAC with timing information.

When the Bt445 is configured for using VIDCLK for loading pixel data, SYNC* and BLANK* correspond to the pixel data being loaded on the same clock edge.

Every clock cycle, the selected color information from the color palette RAMs or overlay registers are presented to the D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 6 and 7.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) may contain sync information. Tables 2 and 3 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the the Bt445 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

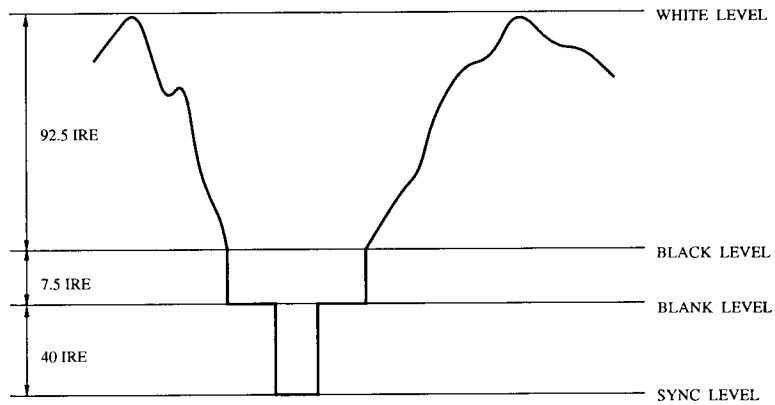

Figure 6. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 2. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
18.6	0.698	26.67	1.00
0.00	0.000	8.05	0.302
0.00	0.000	0.00	0.000

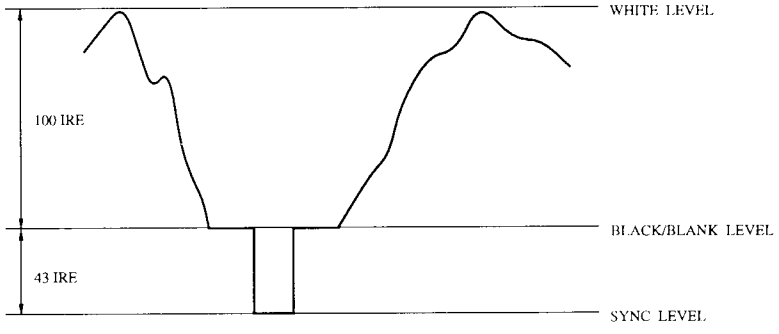

Figure 7. Composite Video Output Waveform SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.5	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 3. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

Frame Buffer Interface

Systems Using VIDCLK* for Loading Pixel Data

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt445 incorporates internal registers and multiplexers. As illustrated in Figure 8, on the rising edge of LD/SCLKI and VIDCLKI, sync and blank information, color, overlay, cursor, and palette bypass information are all registered. The number of pixels supplied for each input cycle depends on the multiplex rate as determined by the current mode. Note that with this configuration, the sync and blank timing will be recognized only with load pixel rate resolution, set by the multiplex mode. Typically, the LD/SCLKI signal is generated from the inverted signal of the VIDCLK* output of the Bt445.

Pixel port bits used as overlay inputs have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

LD/SCLKI may be phase shifted in any amount relative to CLOCK or VIDCLK*. As a result, the pixel and overlay data are registered on the rising edge of LD/SCLKI, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD/SCLKI signal by at least one, but not more than TBD, clock cycles. This LOAD signal transfers the registered pixel and overlay data into a second set of registers, which are then internally multiplexed at the pixel clock rate.

Color Selection

At each pixel port load cycle, one or more pixels consisting of color, overlay, cursor, and/or palette bypass information are processed by the multiplexing and unpacking logic, read masks, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

The color selection process may be broken down into the following steps:

1. Multiplex the input pixels from the pixel port load cycle to the pixel clock rate using the appropriate pixel port start position, pixel unpacking mode, and pixel multiplex mode.
2. Expand the resulting 1:1 pixel data to 8 bits each of red, green, and blue; 4 bits of overlay; 2 bits of

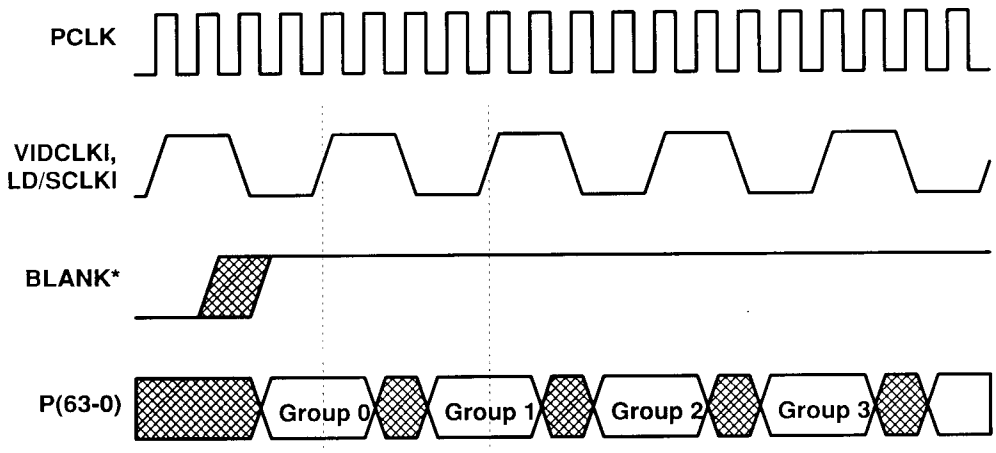

*Figure 8. Frame Buffer and Pixel Port Timing Diagram, Using VIDCLK*Output.*

cursor; and 1 bit of palette bypass control. Pseudo-color modes will supply the same 8-bit result to each of the red, green, and blue colors at this point.

3. Apply the appropriate read masks to the pixel data.
4. Apply the appropriate blink masks to the pixel data.
5. If the palette is bypassed apply the resulting pixel data directly to the DAC inputs; otherwise, apply the pixel data to the addresses of each of the respectively red, green, and blue color palettes. Use the results to drive the DACs inputs.

Pixel Port Start Position Selection

The Bt445's pixel path architecture allows the configurability of the starting position for pixel unpacking. This provides the system designer with greater options to tailor the Bt445 to the desired frame buffer organization. The starting position is configured via the Pixel Port Start Position Register and may be specified to be any position from P(63) to P(0).

One use could be in systems utilizing double frame buffer designs. For example, in an MSB unpacking, 8-bit pixel, 4:1 multiplex configuration, frame buffer A could be attached to input pixel port bits P(31–0) and frame buffer B could be attached to input pixel port bits P(63–32). Assuming the other registers have been appropriately programmed, the Bt445 would allow switching between the frame buffers by simply programming a $20 (for frame buffer A) or a $40 (for frame buffer B) into the Pixel Port Start Position Register.

Pixel Unpacking Selection

The Bt445 supports pixel unpacking starting from either the low-order side of the input pixel port (LSB unpacking) or the high-order side of the input pixel port (MSB unpacking). The starting bit for either unpacking direction is specified by using the Pixel Port Start Position Register. For further information, see the Pixel Port Start Position Register in the Internal Register section. Within each pixel, the MSB is the highest numbered bit.

Pixel Depth Selection

The Bt445 provides extremely flexible options for various pixel depths on a frame-by-frame basis. The selection of the pixel depth is set via the Pixel Depth Register. The pixel depth may be specified to be any size from 1–32 bits per pixel. Not all bits of a pixel will necessarily be used. The pixel depth must be consistent with the pixel port start position and multiplex rate.

Multiplex Rate Selection

The Multiplex Rate is selectable independent from the pixel depth and pixel port start position. Valid multiplex rates are 1:1 to 64:1 (any integer amount). Again, the only restriction is that the multiplex rate must be consistent with the pixel depth and pixel port start position. When using VIDCLK to load pixels, the multiplex rate should be programmed at the same rate as the VIDCLK* rate to select the cycle time of VIDCLK*.

Start Position/Pixel Depth/Multiplex Rate Restrictions

The Bt445 is specified to operate at the pixel depths, pixel port start positions, and multiplex rates that satisfy the following relationship:

For MSB unpacking:
$$\text{Start Position} - (\text{Pixel Depth} \times \text{Multiplex Rate}) \geq 0$$

For LSB unpacking:
$$(\text{Pixel Depth} \times \text{Multiplex Rate}) - \text{Start Position} \leq 64$$

Programming the Bt445 to configurations not consistent with this relationship will yield unspecified results that will not be tested or guaranteed.

Pixel Processing

The pixel unpacking process, which uses the pixel port start position, pixel depth, and multiplex rate, internally yields a serialized pixel stream. Each pixel in this serial stream may be up to 32 bits wide, as specified by the Pixel Depth Register. At this point, the individual fields are extracted from each pixel. The fields extracted are: Red, Green, Blue, Overlay, Cursor, and Palette Bypass Control. The red, green, and blue fields may each be up to 8 bits wide, the overlay field may be up to 4 bits wide, and the palette bypass control may be 1 bit wide. The MSB position and width of each of these fields within the pixel is independently specified by the corresponding source and width registers. The fields may overlap or be noncontiguous. For example, for 8-bit pseudo color mode, the red, green, and blue position and width registers would specify the same field of the pixel.

5-Bit Input Pixel Field		High-order Bits of Input Pixel to be Low-Order Appended	Resulting 8-bit Expanded Field
Hex	Binary		
$00	0 0000	000	$00
$01	0 0001	000	$08
$02	0 0010	000	$10
$03	0 0011	000	$18
$04	0 0100	001	$21
$05	0 0101	001	$29
$06	0 0110	001	$31
$07	0 0111	001	$39
$08	0 1000	010	$42
$09	0 1001	010	$4A
$0A	0 1010	010	$52
$0B	0 1011	010	$5A
$0C	0 1100	011	$63
$0D	0 1101	011	$6B
$0E	0 1110	011	$73
$0F	0 1111	011	$7B
$10	1 0000	100	$84
$11	1 0001	100	$8C
$12	1 0010	100	$94
$13	1 0011	100	$9C
$14	1 0100	101	$A5
$15	1 0101	101	$AD
$16	1 0110	101	$B5
$17	1 0111	101	$BD
$18	1 1000	110	$C6
$19	1 1001	110	$CE
$1A	1 1010	110	$D6
$1B	1 1011	110	$DE
$1C	1 1100	111	$E7
$1D	1 1101	111	$EF
$1E	1 1110	111	$F7
$1F	1 1111	111	$FF

If this effect is not desired, the read mask registers may be used to force the appended LSBs to zero.

Table 4. Expansion of Pixel Color Fields Less Than 8 Bits to an 8-bit Field. Five-bit Pixel Color Field Example.

Generation of Unspecified Pixel Data LSBs

When true-color source pixel data contains less than 8 bits per color channel, it is expanded to 8 bits by left justifying and adding the appropriate LSBs to allow for full-scale and best-fit linearity over the DAC output range. This allows the use of the same gamma correction table for the various pixel modes. Table 4 illustrates this effect by indicating the actual values applied to the red DAC input when in the 16-bit-per-pixel 5-5-5 mode, with palette bypass.

Circuit Description *(continued)*

Color Palette Bypass Mode

The color palette bypass control is used to control the access to the color palette RAM by the pixel data. The overlay and cursor color palette are not affected; they are always used if overlay or cursor data is present. Bypassing the color palette delivers what would have been the palette address directly to the DAC inputs.

Blinking

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt445 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining the number of syncs per blanking time. The Bt445 assumes that a vertical retrace occurs whenever more than one sync occurs during a blank interval.

Systems that do not require separate sync for the digital output section may provide a composite sync input on the SYNC*/HSYNC* input pin; the VSYNC* input should be a logical one. The Bt445 generates composite SYNC* by logically ORing the SYNC*/HSYNC* input with the VSYNC* input.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM.

Pixel Output Interface

The digital pixel output interface can be operated in either of two true-color modes: 4-4-4 or 8-8-8. This interface also provides the pixel output clock (PCLK), pipelined sync (PSYNC*) and pipelined blank (PBLANK*) outputs, and 12 bits of data. The pixel output interface signals OR(3–0), OG(3–0), OB(3–0), and PCLK are specified to run at a maximum pixel rate of 55 MHz when in 4-4-4 mode, or 27.5 MHz when in 8-8-8 mode (see Figure 9).

4-4-4 True-Color Mode

When operated in 4-4-4 true-color mode, the pixel output interface provides 12 bits of pixel data, (one pixel) on each rising or falling edge of the pixel clock output, where each group of 4 bits corresponds to the most significant nibble of the 3 bytes being provided at the red, green, and blue DAC inputs. OR(3–0) carries the R(7–4), OG(3–0) carries G(7–4), and OB(3–0) carries B(7–4).

8-8-8 True-Color Mode

When operated in 8-8-8 true-color mode, the pixel output interface provides 24 bits of pixel data each PCLK cycle. Each edge of the pixel data carries 12 bits of the pixel data, first the high order nibbles of red,

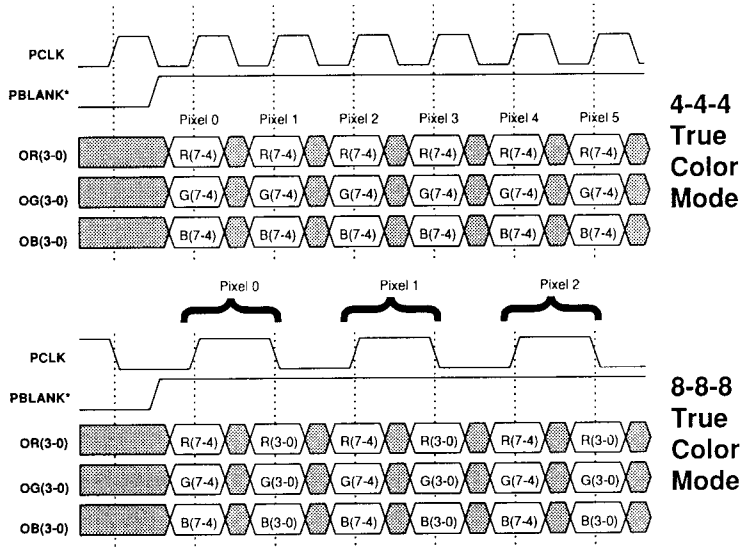

Figure 9. Pixel Output Interface Modes Representative Timing Diagram.

Circuit Description *(continued)*

green, and blue are presented on the rising edge of the pixel clock, then the low-order nibbles are presented on the falling edge of the clock. Note that decreased horizontal spacial resolution is traded for increased color resolution.

Reset Initialization

The S0 and S1 inputs are used at reset time to load the PLL Control Register with the proper CPU output clock multiplex rate. This allows for immediate proper selection of the CPU clock rate. While RESET* is a logical zero, the S0 and S1 inputs flow through and are latched as RESET* rises. The CPU output clocks are also glitchless during transitions as defined for VID-CLK rate transitions.

Power-Down Mode

The Bt445 incorporates a power-down capability, controlled by command bits CR13 and CR14. While both command bits are a logical zero, the Bt445 functions in the normal operating mode.

The command bits can be set so that the DACs and power to the RAM are turned off. Note that the RAM still retains the data. The RAM may be read by or written through the MPU. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. The DACs output no current, and the command registers may still be written to or read by the MPU. Note that the output DACs require about 1 second to turn off (sleep mode) or turn on depending on the compensation capacitor.

In order to conserve power during TFT-only operation, the DACs can be turned off, shunting valid pixel data to the TTL outputs. During this operation, the RAM is still active, indexing pixel data to RGB values.

Boundary Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt445 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to IEEE P1149.1, *Standard Test Access Port and Boundary Scan Architecture*, the Bt445 has dedicated pins which are used for test purposes only.

JTAG uses boundary-scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a Boundary-Scan Register (BSR), which applies or captures test data used for functional verification of the RAMDAC. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select) TCK (Test Clock), TDI (Test Data Input) and TDO (Test Data Out). Complete verification of the RAMDAC can be achieved through these four TAP pins. With boundary-scan cells at each digital pin, the Bt445 is able to apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt445 from the other components on the board, the user has easy access to all Bt445 digital pins through the TAP and can perform complete functionality testing without using expensive bed-of-nails testers.

The bidirectional MPU port and all digital outputs require extra attention with respect to JTAG. Because JTAG requires full control over each digital pin, additional output enable (OE) cells are included in the BSR for the MPU I/O port and various digital outputs. When loaded by the JTAG instructions, these OE cells control the driving strength of their respective pins.

With the JTAG bus, users also have access to a vital portion of the Bt445, the Signature Analysis Register (see Figure 10). With access to this register, users can easily verify expected video data serially through the JTAG port. The SAR is located between the lookup table and the inputs to the DACs.

With the power-on reset (POR) circuitry, the Bt445 will initialize each pin to operate in a RAMDAC mode instead of a JTAG test mode during power-up sequence.

Circuit Description *(continued)*

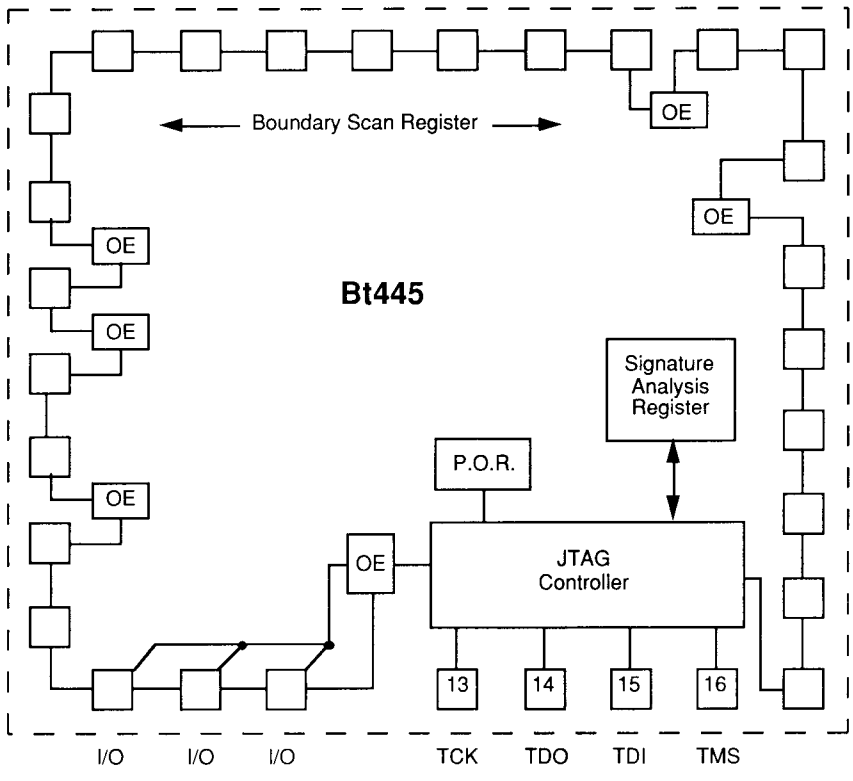

Figure 10. JTAG Block Diagram.

Internal Registers

The following are important programming notes regarding future code compatibility:

- Internal reserved address locations should not be accessed.
- To ensure compatibility with future Bt445 code-compatible devices, reserved values for fields should never be written.
- To ensure compatibility with future Bt445 code-compatible devices, reserved bits should be maintained with read-modify-writes, which only update the unreserved bits. Furthermore, when testing the contents of internal registers, reserved fields should be ANDed off prior to making comparisons. Although it should not be assumed that these reserved bits will always return zeros when read, the reset values will always be as shown.
- It is recommended that the lower 2 bits of overlay blink-and-read mask values be read and/or written from the extended register space (i.e., C(2)=1). Although functionally equivalent to accesses from the Bt458-compatible address space, new code will be easier to modify for future Bt445 code-compatible devices if these accesses are made in the extended register space.

Internal Registers *(continued)*

Command Register 0

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Reserved (logical zero)	0	In the Bt458, this bit specifies 4:1 multiplex mode. In the Bt445, this bit is ignored. To configure the Bt445 for Bt458-compatible 5:1, the extended Bt445 register set must be used.
6	Overlay color 0 disable (0) Use overlay color 0 (1) Use color palette RAM	1	When the overlay select bits are 0000, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
5,4	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	00	These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).
3	Overlay Plane 1 blink enable (0) Disable blinking (1) Enable blinking	0	If a logical one, this bit forces the overlay bit 1 inputs, if any, to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the overlay bit 1 inputs. This bit is also mapped into the Overlay Blink Enable Register bit 1.
2	Overlay Plane 0 blink enable (0) Disable blinking (1) Enable blinking	0	If a logical one, this bit forces the overlay bit 0 inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the overlay bit 0 inputs. This bit is also mapped into the Overlay Blink Enable Register bit 0.
1	Overlay plane 1 display enable (0) Disable (1) Enable	1	If a logical zero, this bit forces the overlay plane 1 inputs, if any, to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the overlay plane 1 input. This bit is also mapped into the Overlay Display Enable Register bit 1.
0	Overlay plane 0 display enable (0) Disable (1) Enable	1	If a logical zero, this bit forces the overlay plane 0 inputs, if any, to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the overlay plane 0 input. This bit is also mapped into the Overlay Display Enable Register bit 0.

Internal Registers *(continued)*

Command Register 1

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Green sync enable (0) Disable sync on IOG (1) Enable sync on IOG	0	This bit enables or disables sync information from being generated on the IOG output.
6	Pedestal Enable (0) 0 IRE (1) 7.5 IRE	1	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. A 0 IRE specifies that the black and blank levels are the same.
5	Reserved	0	Reserved for future expansion.
4,3	Power Down Enable (00) Normal Operation (01) DACs off (10) DACs and RAM off (11) Disable Internal Clocking	00	While these bits are 00, the device operates normally. With the DACs off standard operation occurs, but the output of the LUT is routed directly to the TTL outputs. If these register bits are set for the DACs and power to the RAM is turned off, functional operation is discontinued. In both power-down modes, the RAM still retains the data, and CPU reads and writes can occur with no loss of data. While the device is in the disable internal clocking mode, the internal clock and other output clock modes are completely disabled to further conserve power when in power-down mode. The RAM still retains the data and MPU reads and writes can occur with no loss of data.
2	Palette Addressing Mode (0) Sparse (1) Contiguous	0	This bit controls the field expansion mode. When this bit is a logical zero, pixel fields containing fewer than the normal width of the field will be expanded by left justifying the specified bits and using group replication onto the unspecified lower bits. When this bit is a logical one, the specified bits will be right justified with zeros placed onto the unspecified MSBs.
1	Signature Analysis Enable (0) Disable SAR (1) Enable SAR	0	This bit enables operation of all signature analysis register (SAR) clocking. A logical zero is the normal mode, the SAR disabled. Writing a logical one enables the SAR for operation on every pixel. As slightly more power is consumed when the SAR is enabled, it is recommended that the SAR be disabled when not actually being used.
0	Reset Pipelined Depth	0	Transitioning this bit from a logical zero to a logical one causes the pixel pipeline depth to be initialized. For further information, see "Pipeline Delay Initialization" in the Applications section.

Internal Registers *(continued)*

Red MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$07	Position of the MSB of the red field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the red color palette or red DAC output. The value specified should be less than the pixel size.

Red Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits : ($08)–8 Bits ($09)–Reserved : ($FF)–Reserved	$08	Number of bits to be used for the red field in a pixel. The size and position of the red field must lie within the defined pixel size.

Red Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–0	Blink Enable	$00	Bits 7–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) pixel planes 7–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. The register is also written with MPU data whenever the Bt458-compatible blink register is written.

Internal Registers *(continued)*

Red Display Enable Control

This register is also written when the Bt458-compatible read mask register is written.

Bit(s)	Field Name	Reset Value	Field Description
7	Enable Bit Plane 7 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 7. A logical zero causes bit 7 of the red field of the pixel to be forced to zero. A logical one causes bit 7 of the red field to pass to the color palette or DAC.
6	Enable Bit Plane 6 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 6. A logical zero causes bit 6 of the red field of the pixel to be forced to zero. A logical one causes bit 6 of the red field to pass to the color palette or DAC.
5	Enable Bit Plane 5 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 5. A logical zero causes bit 5 of the red field of the pixel to be forced to zero. A logical one causes bit 5 of the red field to pass to the color palette or DAC.
4	Enable Bit Plane 4 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 4. A logical zero causes bit 4 of the red field of the pixel to be forced to zero. A logical one causes bit 4 of the red field to pass to the color palette or DAC.
3	Enable Bit Plane 3 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 3. A logical zero causes bit 3 of the red field of the pixel to be forced to zero. A logical one causes bit 3 of the red field to pass to the color palette or DAC.
2	Enable Bit Plane 2 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 2. A logical zero causes bit 2 of the red field of the pixel to be forced to zero. A logical one causes bit 2 of the red field to pass to the color palette or DAC.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 1. A logical zero causes bit 1 of the red field of the pixel to be forced to zero. A logical one causes bit 1 of the red field to pass to the color palette or DAC.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of red bit plane 0. A logical zero causes bit 0 of the red field of the pixel to be forced to zero. A logical one causes bit 0 of the red field to pass to the color palette or DAC.

Internal Registers *(continued)*

Green MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$07	Position of the MSB of the green field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the green color palette or green DAC output. The value specified should be less than the pixel size.

Green Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits : ($08)–8 Bits ($09)–Reserved : ($FF)–Reserved	$08	Number of bits to be used for the green field in a pixel. The size and position of the green field must lie within the defined pixel size.

Green Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–0	Green Blink Enable	$00	Bits 7–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) green pixel planes 7–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. The register is also written with MPU data whenever the Bt458-compatible blink register is written.

Internal Registers *(continued)*

Green Display Enable Control

This register is also written mapped to the Bt458-compatible read mask.

Bit(s)	Field Name	Reset Value	Field Description
7	Enable Bit Plane 7 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 7. A logical zero causes bit 7 of the green field of the pixel to be forced to zero. A logical one causes bit 7 of the green field to pass to the color palette or DAC.
6	Enable Bit Plane 6 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 6. A logical zero causes bit 6 of the green field of the pixel to be forced to zero. A logical one causes bit 6 of the green field to pass to the color palette or DAC.
5	Enable Bit Plane 5 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 5. A logical zero causes bit 5 of the green field of the pixel to be forced to zero. A logical one causes bit 5 of the green field to pass to the color palette or DAC.
4	Enable Bit Plane 4 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 4. A logical zero causes bit 4 of the green field of the pixel to be forced to zero. A logical one causes bit 4 of the green field to pass to the color palette or DAC.
3	Enable Bit Plane 3 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 3. A logical zero causes bit 3 of the green field of the pixel to be forced to zero. A logical one causes bit 3 of the green field to pass to the color palette or DAC.
2	Enable Bit Plane 2 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 2. A logical zero causes bit 2 of the green field of the pixel to be forced to zero. A logical one causes bit 2 of the green field to pass to the color palette or DAC.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 1. A logical zero causes bit 1 of the green field of the pixel to be forced to zero. A logical one causes bit 1 of the green field to pass to the color palette or DAC.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of green bit plane 0. A logical zero causes bit 0 of the green field of the pixel to be forced to zero. A logical one causes bit 0 of the green field to pass to the color palette or DAC.

Internal Registers *(continued)*

Blue MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$07	Position of the MSB of the blue field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the blue color palette or blue DAC output. The value specified should be less than the pixel size.

Blue Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits : ($08)–8 Bits ($09)–Reserved : ($FF)–Reserved	$08	Number of bits to be used for the blue field in a pixel. The size and position of the blue field must lie within the defined pixel size.

Blue Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–0	Blue Blink Enable	$00	Bits 7–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) blue pixel planes 7–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. The register is also written with MPU data whenever the Bt458-compatible blink register is written.

Internal Registers *(continued)*

Blue Display Enable Control

This register is also written when the Bt458-compatible read mask register is written.

Bit(s)	Field Name	Reset Value	Field Description
7	Enable Bit Plane 7 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 7. A logical zero causes bit 7 of the blue field of the pixel to be forced to zero. A logical one causes bit 7 of the blue field to pass to the color palette or DAC.
6	Enable Bit Plane 6 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 6. A logical zero causes bit 6 of the blue field of the pixel to be forced to zero. A logical one causes bit 6 of the blue field to pass to the color palette or DAC.
5	Enable Bit Plane 5 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 5. A logical zero causes bit 5 of the blue field of the pixel to be forced to zero. A logical one causes bit 5 of the blue field to pass to the color palette or DAC.
4	Enable Bit Plane 4 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 4. A logical zero causes bit 4 of the blue field of the pixel to be forced to zero. A logical one causes bit 4 of the blue field to pass to the color palette or DAC.
3	Enable Bit Plane 3 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 3. A logical zero causes bit 3 of the blue field of the pixel to be forced to zero. A logical one causes bit 3 of the blue field to pass to the color palette or DAC.
2	Enable Bit Plane 2 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 2. A logical zero causes bit 2 of the blue field of the pixel to be forced to zero. A logical one causes bit 2 of the blue field to pass to the color palette or DAC.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 1. A logical zero causes bit 1 of the blue field of the pixel to be forced to zero. A logical one causes bit 1 of the blue field to pass to the color palette or DAC.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of blue bit plane 0. A logical zero causes bit 0 of the blue field of the pixel to be forced to zero. A logical one causes bit 0 of the blue field to pass to the color palette or DAC.

Internal Registers *(continued)*

Overlay MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$09	Position of the MSB of the overlay field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the overlay palette or all DAC outputs. The value specified should be less than the pixel size.

Overlay Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits ($03)–3 Bits ($04)–4 Bits ($05)–Reserved : ($FF)–Reserved	$02	Number of bits to be used for the overlay field in a pixel. The size and position of the overlay field must lie within the defined pixel size.

Overlay Blink Enable Register

Bit(s)	Field Name	Reset Value	Field Description
7–4	Reserved	$0	Reserved for future expansion.
3–0	Overlay Blink Enable	$0	Bits 3–0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) overlay pixel planes 3–0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic. Bits 0 and 1 of this field are also read and written by accessing the Bt458-compatible overlay blink controls in Command Register 0.

Internal Registers *(continued)*

Overlay Display Enable Control

Bits 1 and 0 of this register are also mapped to the Bt458-compatible command register 0 bits 1 and 0.

Bit(s)	Field Name	Reset Value	Field Description
7–4	Reserved	0	Reserved for future expansion.
3	Enable Bit Plane 3 (0) Disable (1) Enable	0	This bit controls the enabling of overlay bit plane 3. A logical zero causes bit 3 of the overlay field of the pixel to be forced to zero. A logical one causes bit 3 of the overlay field to pass to the overlay palette.
2	Enable Bit Plane 2 (0) Disable (1) Enable	0	This bit controls the enabling of overlay bit plane 2. A logical zero causes bit 2 of the overlay field of the pixel to be forced to zero. A logical one causes bit 2 of the overlay field to pass to the overlay palette.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of overlay bit plane 1. A logical zero causes bit 1 of the overlay field of the pixel to be forced to zero. A logical one causes bit 1 of the overlay field to pass to the overlay palette.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of overlay bit plane 0. A logical zero causes bit 0 of the overlay field of the pixel to be forced to zero. A logical one causes bit 0 of the overlay field to pass to the overlay palette.

Internal Registers *(continued)*

Cursor MSB Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	MSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$00	Position of the MSB of the cursor field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to access the cursor palette or all DAC inputs. The value specified should be less than the pixel size.

Cursor Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–2 Bits ($03)–Reserved : ($FF)–Reserved	$02	Number of bits to be used for the cursor field in a pixel. The size and position of the cursor field must lie within the defined pixel size.

Cursor Blink Register

Bit(s)	Field Name	Reset Value	Field Description
7–2	Reserved	000000	Reserved for future expansion.
1, 0	Cursor Blink Enable	00	Bits 1 and 0, corresponding to the expanded (i.e., either right justified and zero padded, or left justified and MSB replicated) cursor pixel planes 1 and 0, respectively, enable blinking of individual planes. A logical one in any bit position causes the corresponding pixel plane to be turned off in accordance with the blink rate counter and duty cycle. A logical zero causes the corresponding pixel plane to be unaffected by the blink logic.

Internal Registers *(continued)*

Cursor Display Enable Control

Bit(s)	Field Name	Reset Value	Field Description
7–2	Reserved	0000000	Reserved for future expansion.
1	Enable Bit Plane 1 (0) Disable (1) Enable	1	This bit controls the enabling of cursor bit plane 1. A logical zero causes bit 1 of the cursor field of the pixel to be forced to zero. A logical one causes bit 1 of the cursor field to pass to the cursor palette.
0	Enable Bit Plane 0 (0) Disable (1) Enable	1	This bit controls the enabling of cursor bit plane 0. A logical zero causes bit 0 of the cursor field of the pixel to be forced to zero. A logical one causes bit 0 of the cursor field to pass to the cursor palette.

Palette Bypass Position

Bit(s)	Field Name	Reset Value	Field Description
7–0	LSB Position ($00)–Pixel Bit 0 ($01)–Pixel Bit 1 : ($1F)–Pixel Bit 31 ($20)–Reserved : ($FF)–Reserved	$00	Position of the LSB of the palette bypass field within the input pixel. This field, in conjunction with the size, determines which bits of the input pixel are used to control palette bypass. The value specified should be less than the pixel size.

Palette Bypass Width Control

Bit(s)	Field Name	Reset Value	Field Description
7–0	Size ($00)–Reserved ($01)–1 Bit ($02)–Reserved : ($FF)–Reserved	$01	Number of bits to be used for the palette bypass field in a pixel. The size and position of the palette bypass field must lie within the defined pixel size.

Internal Registers *(continued)*

Pixel Port Start Position Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Definition	Reset Value	Description
7–0	Pixel Port Start Position ($00) Bit 0 ($01) Bit 1 : ($3F) Bit 63 ($40) Bit 64 ($41) Reserved : ($FF) Reserved	$28	When MSB unpacked, this register should be loaded with the MSB + 1 of the pixel input bits to be used. When LSB unpacked, This register contains the LSB number of the pixel bits to be used. For example, if MSB unpacking is desired using bits 31–0 of the input pixel port, then this register should be loaded with $20. This register selects the starting bit position for the pixel unpacking logic.

Internal Registers *(continued)*

Pixel Format Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Definition	Reset Value	Description
7	Pixel Unpacking Order (0) MSB Unpacking (1) LSB Unpacking	0	This bit selects the pixel unpacking ordering. When pixels are MSB unpacked, the first pixel output will come from the higher-order bits of the input pixel port. When LSB is unpacked, the first pixel output will come from the lower-order bits of the input pixel port.
6	Reserved	0	Reserved for future expansion.
5	Cursor Enable (0) Disable (1) Enable	0	This bit enables the input pixel cursor field to select the cursor palette. When this bit is a logical zero, the input pixel cursor field is ignored.
4	Cursor Color 0 Enable (0) Disable (1) Enable	0	This bit enables the use of cursor color 0. When this bit is a logical zero, a cursor field value of zero causes the cursor to be transparent. When this bit is a logical one, a cursor field value of zero causes cursor color 0 to be used.
3	Overlay Enable (0) Disable (1) Enable	1	This bit enables the input pixel overlay field to select the overlay palette. When this bit is a logical zero, the input pixel overlay field is ignored.
2	Reserved	0	Reserved for future expansion.
1, 0	Palette Bypass Control (00) Always use Color Palette (01) Always bypass Color Palette (10) Use input pixel field (11) Reserved	00	This field specifies how the pixel data should address the color palette, or bypass it. If the color palette is used, a pixel will address the color palettes, and its contents would then be used as the inputs to the DACs or to drive the pixel output port. Cursor and overlays always use the color palette.

Internal Registers *(continued)*

Pixel Depth Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7–0	Pixel Depth Select ($00) Reserved ($01) 1 Bit/Pixel ($02) 2 Bits/Pixel ($03) 3 Bits/Pixel : ($1E) 30 Bits/Pixel ($1F) 31 Bits/Pixel ($20) 32 Bits/Pixel ($21) Reserved : ($FF) Reserved	$0A	These bits select the pixel depth. The total number of bits per pixel, including overlay, cursor, and unused bits in each pixel, must be specified. The reset value is consistent with the Bt458 (10 bits per pixel, 8 pseudo color plus 2 overlay).

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Pixel PLL Rate Register 0

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Reserved (logical zero)	00	Reserved.
5–0	Multiplier Selection (M) ($00) Reserved : ($17) Reserved ($18) Multiply by 24 ($19) Multiply by 25 : ($3E) Multiply by 62 ($3F) Multiply by 63	011001	Determines the multiplier factor for the input oscillator frequency (M) used in determining the final pixel clock frequency.

Internal Registers *(continued)*

Pixel PLL Rate Register 1

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Pixel Clock Divider (L) (00) Divide by 1 (01) Divide by 2 (10) Divide by 4 (11) Divide by 8	00	This bit controls the Pixel PLL divider L.
5,4	Reserved	00	Reserved.
3–0	Pixel Clock Divisor Selection (N) (0000) Reserved (0001) Reserved : (0011) Divide by 4 (0100) Divide by 5 : (1110) Divide by 15 (1111) Reserved	0100	Determines the divisor factor for the input oscillator frequency (N) used in determining the final pixel clock frequency.

Internal Registers *(continued)*

PLL Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Pixel Clock PLL Enable (0) PLL Disable (1) PLL Enable	1	This bit determines whether the PLL used to generate the pixel clock should be enabled or disabled. Should the PLL be disabled, the pixel clock must be input via the CLOCK and CLOCK*.
6	MCLK Enable (0) MCLKs Disabled (1) MCLKs Enabled	1	This bit disables the PLL used to synthesize the master clock which eventually generates the CPU clock, 20 MHz and 25 MHz clock. A logical zero written to this bit disables (i.e., three-states) PLL operation for these clocks only.
5,4	CPU Clock Selection (00) 50 MHz (01) 40 MHz (10) 33 MHz (11) 25 MHz	S(1,0)	These bits select the CPU frequency for CPUCLK output. When RESET* is active, S1 and S0 select the initial values of these two bits; when RESET* rises, these bits are latched.
3–0	VCO Gain Control (0000)–Range 0 (0001)–Range 1 (0010)–Range 2 : (0111)–Range 7 (1000)–Range 8 : (1111)–Range 15	1000	PLL VCO Gain Control.

Internal Registers *(continued)*

VIDCLK Cycle Control Register*

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Reserved	00	Reserved for future expansion.
5–0	VIDCLK Cycle Time Select (000000) CLOCK (000001) CLOCK/2 (000010) CLOCK/3 (000011) CLOCK/4 : (111101) CLOCK/62 (111110) CLOCK/63 (111111) CLOCK/64	000011	These bits select the VIDCLK* cycle time in pixel clock units.

Internal Registers *(continued)*

Pixel Load Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7–5	Reserved	000	Reserved
4	SCLK* Control (0) Extra pulse not needed (1) Extra pulse needed	0	This bit specifies whether the first SCLK* pulse after a blanked time is needed (logical one) to read the first pixel item. A logical zero indicates that the system has externally provided the first VRAM shift clock, and the Bt445 may register valid pixel data with the first SCLK*.
3	SCLK* Enable (0) SCLK* Disabled (1) SCLK* Enabled	0	A logical one must be written to this bit to enable SCLK* to be output. A logical zero written to this bit three-states the SCLK* output and the system should use VIDCLK* to generate LD/SCLKI.
2	VIDCLK* Enable (0) VIDCLK* Disabled (1) VIDCLK* Enabled	1	A logical one must be written to this bit to enable VIDCLK to be output. A logical zero written to this bit three-states the VIDCLK* output.
1, 0	Reserved (logical zero)	00	Reserved.

Internal Registers *(continued)*

Digital Output Control Register

The command register may be written to or read by the MPU at any time. Bit 0 corresponds to data bus bit D0.

Bit(s)	Field Name	Reset Value	Field Description
7	Operating Mode (0) 4-4-4 True Color (1) 8-8-8 True Color	0	This bit selects the 4-4-4 or 8-8-8 true-color mode. When this bit is a logical zero, the 4-4-4 mode of operation is selected. In this mode the appropriate PCLK edge delivers the high-order nibble of the data being delivered to the DAC inputs. When this bit is a logical one, the 8-8-8 mode of operation is selected. In this mode the high-order nibble of each pixel is delivered on each PCLK rising edge, and the low-order nibble of each pixel is delivered on the falling edge of PCLK. In 8-8-8 mode, the PCLK edge select control is not used.
6	Reserved	0	Reserved.
5	OR, OG, OB(3–0) Output Enable (0) Disable (1) Enable	0	This bit enables the red, green, and blue digital outputs. This output should not be enabled when the pixel rate exceeds that specified by the AC timing parameters for this output. A logical zero in this bit disables (i.e., three-states) the red, green, and blue digital outputs. When three-stated, these outputs will float to valid TTL levels since internal pullup resistors are provided.
4	PVSYNC*, PHSYNC* Output Enable (0) Disable (1) Enable	0	This bit enables the separate pipelined sync outputs. A logical one enables the outputs; a logical zero causes these outputs to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.
3	PSYNC* Output Enable (0) Disable (1) Enable	0	This bit enables the pixel-synchronized, pipelined sync output signal. It may be used to generate the TTL sync signal required by monitors having separate sync. A logical one enables the output; a logical zero causes this output to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.
2	PBLANK* Output Enable (0) Disable (1) Enable	0	This bit enables the pixel-synchronized, pipelined blank output signal. A logical one enables the output; a logical zero causes this output to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.
1	PCLK Edge Select (0) Rising edge (1) Falling edge	0	This bit selects the edge of PCLK to which the digital output changes will be synchronized. A logical zero causes the AC timing parameters for the digital pixel outputs to be referenced to the rising edge of PCLK. A logical one causes the AC timing parameters for the digital pixel outputs to be referenced to the falling edge of PCLK. This bit is not used when the 8-8-8 mode of operation is selected.
0	PCLK Output Enable (0) Disable (1) Enable	0	This bit enables the PCLK output of the digital pixel output port. This output should not be enabled when the pixel rate exceeds that specified by the AC timing parameters for this output. A logical one enables the outputs; a logical zero causes this output to be three-stated. When three-stated, an internal pullup resistor maintains this output at a logical one, provided that it is lightly loaded.

Internal Registers *(continued)*

MPX Rate Register

Bit(s)	Field Name	Reset Value	Field Description
7, 6	Reserved	00	Reserved for future expansion
5–0	MPX Rate ($00) 1:1 ($01) 2:1 ($02) 3:1 ($03) 4:1 : ($3E) 63:1 ($3F) 64:1	$03	Number of pixels loaded per input pixel load cycle. The value specified should be consistent with the pixel depth; i.e. the number of pixels multiplied by the pixel depth less than or equal to the number of bits for which the input port is configured.

Internal Registers *(continued)*

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt445, the value read by the MPU will be $3A. Data written to this register is ignored.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt445. The 4 most significant bits signify the revision letter, A, in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored.

Read Enable Register

Writing this Bt458-compatible register location causes the red, green, and blue read enable registers to be simultaneously written with the MPU data. Each read enable register is used to enable (logical one) or disable (logical zero) red, green, and blue planes from addressing the color palette RAM. D(7–0) correspond to bits 7–0 of the red, green, and blue fields of each pixel, respectively. Each register bit is logically ANDed with the corresponding field bit input. These registers may be written to or read by the MPU at any time and are initialized to $FF. An MPU read of this register reads the contents of the green read enable register.

Blink Enable Register

Writing this Bt458-compatible register location causes the red, green, and blue read blink registers to be simultaneously written with the MPU data. The blink enable register is used to enable (logical one) or disable (logical zero) individual bits in the red, green, and blue color fields from blinking at the blink rate and duty cycle specified by the command register. D(7–0) correspond to field bits 7–0, respectively. In order for a bit plane to blink, the corresponding bit in the read enable register must be a logical one. This register may be written to or read by the MPU at any time and is initialized to $00. An MPU read of this register reads the contents of the Green Blink Enable Register.

Signature Analysis Registers (SAR)

Signature Analysis Operation

These three 8-bit SARs may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the output SARs while BLANK* is a logical zero to load the seed value. The output SARs use data being loaded into the output DACs to calculate the signatures. JTAG logic can access the output SAR independently of the MPU operation. MPU accesses to the SARs require one address register load followed by three reads or writes to the red, green, and blue signature registers, respectively. D0 corresponds to R0, G0, and B0.

By loading a test display into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

It is imperative that the MPU adhere to conditions required to prevent the disruption of pixel data during signature acquisition to ensure consistent results. See the AC Characteristics section for further information.

Test Register 0

The test register provides Bt458-compatible diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is initialized to DAC-select equals none. When writing to the register, the upper 4 bits (D4–D7) are ignored. The contents of the test register are defined in Table 5.

To use test register 0, the host MPU writes to it, selecting the nibble and the DAC input to be read. This specifies which 4 bits of color information the MPU wishes to read (R(3–0), G(3–0), B(3–0), R(7–4), G(7–4), or B(7–4)). When the MPU reads test register 0, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits of the MPU data bus, and the lower 4 bits contain the red, green, blue, low, or high nibble selection information previously written. Note that either the pixel clock must be as slow as the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to test register 0, setting the DAC select field to 001 and the low nibble select to 0. The MPU then reads test register 0, keeping the pixel data stable, which results in D(7–4) containing the R(7–4) DAC input bits, and D(3–0) containing the red, green, blue, low, or high nibble enable information, as illustrated in Table 6.

Data Bit(s)	Field Name	Reset Value	Description
7–4	DAC Input Data	N/A	Color information at DAC input (4 bits of red, green, or blue). Data written to this field is ignored.
3	Low Nibble Select (0) High Nibble (1) Low Nibble	0	Writing a logical one to this field enables the low nibble (i.e., bits 3–0) of the selected DAC input to be read from bits 7–4 of this test register. Writing a logical zero to this field enables the high nibble (i.e., bits 7–4) of the selected DAC inputs to be read from bits 7–4 of this test register.
2–0	DAC Select (000) None (001) Red (010) Green (100) Blue All other decodes are reserved.	000	Blue enable Green enable Red enable

Table 5. Test Register 0.

MPU Bus Bits	Value Read
7–4	R(7–4)
3–0	0001

Table 6. Test Register 0 Example.

Internal Registers *(continued)*

The comparator, which may be accessed in Test Register 1 (see Table 7), enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional. When the monitor is not connected or one of the analog cables connecting the monitor is open (i.e., broken), the voltage present at the corresponding DAC output would be higher than predicted, as one of the termination resistors would not be present.

Bit(s)	Field Name	Reset Value	Description
7, 6	Operand 1 Select (00) Normal Operation (01) Select Green DAC Output (10) Select Red DAC Output (11) Reserved	00	This field selects Operand 1 of the comparator. For normal operation, the operand 1 and 2 fields should both contain 00.
5, 4	Operand 2 Select (00) Normal Operation (01) Select 145 mV Reference (10) Select Blue DAC Output (11) Reserved	00	This field selects Operand 2 of the comparator. For normal operation, the operand 1 and 2 fields should both contain 00.
3	Comparison Result (0) Operand 1 < Operand 2 (1) Operand 1 > Operand 2	N/A	This field yields the result of the comparison of the DAC and/or reference output. Comparing operands whose values lie within a few LSBs will yield unpredictable results. Data written to this bit is ignored, as this field is read only. This result is valid only after the required comparison settling time is reached (i.e., 5 µs after the operand becomes constant).
2–0	Reserved	000	Reserved.

Table 7. Test Register 1.

Pin Descriptions

Pin Count	Pin Name	Description
1	BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as illustrated in Tables 2 and 3. It is registered on the rising edge of LD. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
1	SYNC*/ HSYNC*	Composite sync/Hsync control input (TTL compatible). A logical zero on this input switches off an IRE current source on the IOG output (see Figures 6 and 7). SYNC*/ HSYNC* does not override any other control or data input, as shown in Tables 2 and 3; therefore, it should be asserted only during the blanking interval. It is registered on the rising edge of VIDCLKI. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
1	VSYNC*	Separate sync control inputs (TTL compatible). This signal is registered with each rising edge of VIDCLKI and is pipelined to the pixel data rate, then output with pixel timing to the PVSYNC* outputs. This signal is not internally used by the Bt445.
1	VIDCLKI	Video Clock input (TTL-compatible Schmitt Trigger). The rising edge of this input is used to load the SYNC* and BLANK* control inputs. Also, if SCLK* is not used to control the VRAM frame buffer, pixel inputs (P0–P47) are also loaded with the rising edge of this signal. This input is usually driven with a system-buffered/skewed version of the VIDCLK* output.
1	LD/SCLKI	Load Serial Clock Input (TTL-compatible Schmitt Trigger). This signal is used only when the Bt445 is configured to provide the VRAM serial clock (SCLK*) output. Pixel data is loaded on the rising edge of this signal, except for the first rising edge, which occurs during blanking. This input is usually driven with a system-buffered/skewed version of either the SCLK* output or VIDCLK*.
64	P(63–0)	Pixel Inputs Port (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM, 16 entries of the overlay palette, or 4 entries of cursor palette is to be used to provide color information. Depending on the pixel configuration, up to 64 consecutive pixels per load cycle are input through this port. They are registered on the rising edge of VIDCLKI or LD/SCLKI. These inputs have internal pullup resistors; therefore, unused pins do not require connection. However, if the system configuration allows, the unused pins should be connected to GND.
2	S(1, 0)	CPU Clock Rate Select Switch (TTL compatible). These inputs are used to set the initial CPU clock rate at reset time.
3	IOR, IOG, IOB	Red, green, and blue video current outputs. These high-impedance current sources are capable of directly driving a doubly-terminated 75-Ω coaxial cable (Figure 12).
1	SCLK*	VRAM shift clock output (TTL-voltage-level compatible, low drive). The signal on this pin is equal to the selected pixel clock divided by 1, 2, 4, 8, or 32 depending on the pixel depth selected. This clock must be redriven through an inverting buffer prior to the connection to the serial clock of the VRAMs.
1	VIDCLK*	Video Clock Output (TTL-voltage-level compatible, low drive). This output is a divided pixel as programmed in the VIDCLK* Cycle Control register. This clock must be redriven through an inverting buffer prior to the connection to the CRT timing generation logic.

Pin Descriptions *(continued)*

Pin Count	Pin Name	Description
1	PCLK	Pixel Clock (TTL-voltage-level compatible, low drive). This clock is used to synchronize the next stage with the digital outputs. It must be redriven through a noninverting buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 55 MHz driving a 20 pF load.
1	PSYNC*	Composite SYNC control output (TTL-voltage-level compatible, low drive). This signal is synchronized with the pixel outputs.
2	PHSYNC*, PVSYNC*	Separate SYNC control outputs (TTL-voltage-level compatible, low drive). These signals are synchronized with the pixel outputs.
1	PBLANK*	Composite BLANK control output (TTL-voltage-level compatible, low drive). This signal is synchronized with the pixel outputs.
12	OR (3–0) OG (3–0) OB (3–0)	Digital Outputs (TTL-voltage-level compatible, low drive). These low-drive outputs represent the 4 MSBs of the red, green, and blue DAC decoder and can be used to drive an active matrix TFT directly. These outputs must be redriven through a noninverting buffer prior to the connection to the next stage.
1	CPUCLK	CPU Clock (TTL-voltage-level compatible, low drive). This clock is used to derive the CPU clock and is selectable between 50, 40, 33, and 25 MHz (when using a 20 MHz crystal). This clock must be redriven through a buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 50 MHz driving a 20 pF load.
1	MCLK20	20 MHz Master Clock (TTL-voltage-level compatible, low drive). This master clock generates a constant 20 MHz clock. This clock must be redriven through a buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 50 MHz driving a 20 pF load.
1	MCLK25	25 MHz Master Clock (TTL-voltage-level compatible, low drive). This master clock generates a constant 25 MHz clock. This clock must be redriven through a buffer prior to the connection to the next stage. This pixel clock has a maximum output clock speed of 50 MHz driving a 20 pF load.
1	TMS	Test Mode Select (TTL compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When not performing JTAG operations, this pin should be driven to a logic high.
1	TCK	Test Clock (TTL compatible). Used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When not performing JTAG operations, this pin should be driven to a logic high.
1	TDI	Test Data In (TTL compatible). JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When not performing JTAG operations, this pin should be driven to a logic high.
1	TDO	Test Data Out (TTL compatible). JTAG output used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences, and will be three-stated at all other times. When not performing JTAG operations, this pin should be left floating.

Pin Descriptions *(continued)*

Pin Count	Pin Name	Description
2	COMP, COMP2	Compensation pins. These pins provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between these two pins (Figure 13).
1	FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 13). Note that the IRE relationships in Figures 6 and 7 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = K1 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω) where K1 and K2 are defined as:
1	VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 13. The decoupling capacitor must be as close as possible to the device to keep lead lengths to an absolute minimum.
2	CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
1	XTAL1	Crystal input. This input is either connected to a crystal or driven by a CMOS oscillator. The internal phase lock loops generate the pixel and CPU clocks using this input.
1	XTAL2	Crystal amplifier output. This output is connected to the second terminal of the crystal when used.
1	CE*	Chip enable control input (TTL-compatible Schmitt Trigger). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally registered on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
1	R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is registered on the falling edge of CE*.
3	C(2–0)	Command control inputs (TTL compatible). C2, C1, and C0 specify the type of read or write operation being performed, as illustrated in Table 1. They are registered with the falling edge of CE*.

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

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Pin Descriptions *(continued)*

8	D(7–0)	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
1	RANGE	Compensation for VCO. A 0.01 µF ceramic chip capacitor must be connected between this pin and VAA (Figure 13).
1	RESET*	Reset input (TTL compatible). When this signal is asserted, all the Command Register Bits are set to be in a Bt458-compatible mode.
7	NC	No Connect. Reserved for future expansion. These pins should be left open.
19	VAA	Analog power. All VAA pins must be connected.
11	GND	Analog ground. All GND pins must be connected.

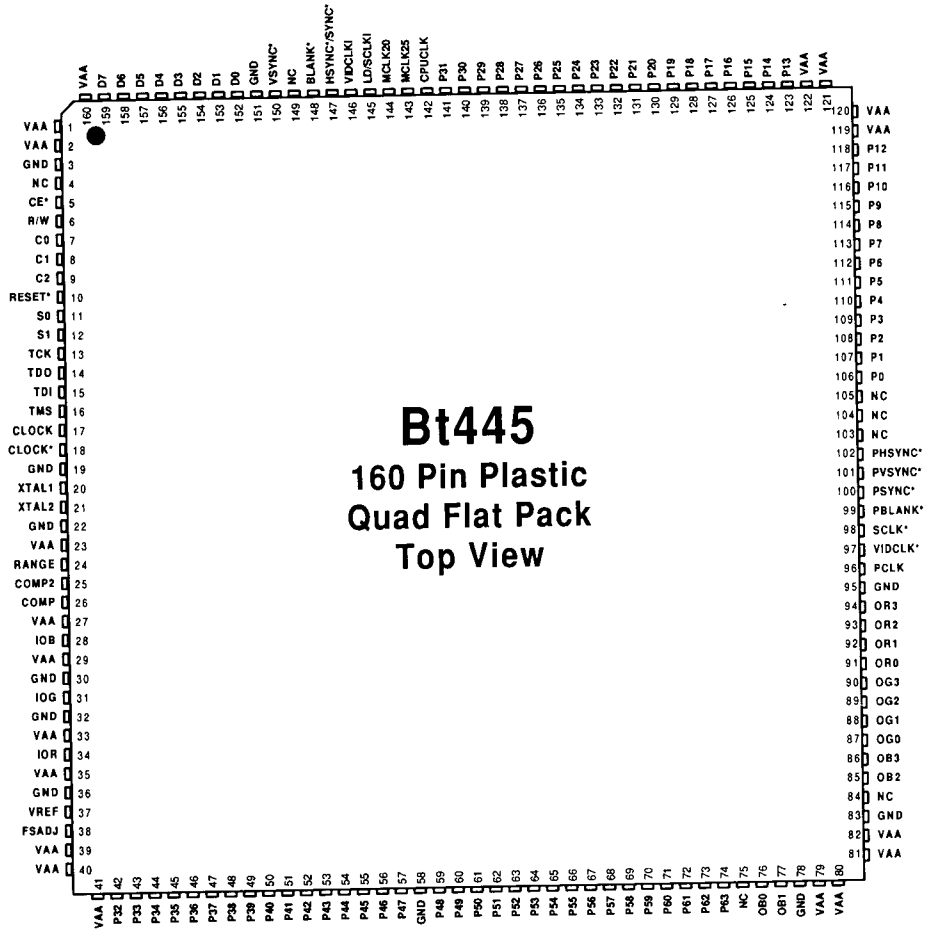


Figure 11. 160-pin PQFP Pin Assignments.

Pin Descriptions *(continued)*

Signal	Pin Number
BLANK*	148
SYNC*/HSYNC*	147
VSYNC*	150
NC	149
CLOCK*	18
CLOCK	17
XTAL1	20
XTAL2	21
RANGE	24
S0	11
S1	12
RESET*	10
CPUCLK	142
MCLK20	144
MCLK25	143
SCLK*	98
VIDCLK*	97
VIDCLKI	146
LD/SCLKI	145
P0	106
P1	107
P2	108
P3	109
P4	110
P5	111
P6	112
P7	113
P8	114
P9	115
P10	116
P11	117
P12	118
P13	123
P14	124
P15	125
P16	126
P17	127
P18	128
P19	129
P20	130
P21	131
P22	132
P23	133
P24	134

Signal	Pin Number
P25	135
P26	136
P27	137
P28	138
P29	139
P30	140
P31	141
P32	42
P33	43
P34	44
P35	45
P36	46
P37	47
P38	48
P39	49
P40	50
P41	51
P42	52
P43	53
P44	54
P45	55
P46	56
P47	57
P48	59
P49	60
P50	61
P5	62
P52	63
P53	64
P54	65
P55	66
P56	67
P57	68
P58	69
P59	70
P60	71
P61	72
P62	73
P63	74
VAA	1
VAA	2
VAA	23
VAA	27
VAA	29
VAA	33
VAA	35

Signal	Pin Number
VAA	39
VAA	40
VAA	41
VAA	79
VAA	80
VAA	81
VAA	82
VAA	119
VAA	120
VAA	121
VAA	122
VAA	160
GND	3
GND	19
GND	22
GND	30
GND	32
GND	36
GND	58
GND	78
GND	83
GND	95
GND	151
NC	4
NC	75
NC	84
NC	103
NC	104
NC	105
PCLK	96
PBLANK*	99
PSYNC*	100
PVSYNC*	101
PHSYNC*	102
OR0	91
OR1	92
OR2	93
OR3	94
OG0	87
OG1	88
OG2	89
OG3	90

Signal	Pin Number
OB0	76
OB1	77
OB2	85
OB3	86
IOR	34
IOG	31
IOB	28
COMP	26
COMP2	25
FS ADJUST	38
VREF	37
CE*	5
R/W	6
C2	9
C1	8
C0	7
D7	159
D6	158
D5	157
D4	156
D3	155
D2	154
D1	153
D0	152
TMS	16
TCK	13
TDI	15
TDO	14

5

PC Board Layout Considerations

PC Board Considerations

The Bt445 layout should be optimized for lowest noise on the Bt445 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground planes must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferable analog ground plane), layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt445 to be located as close as possible to the power supply connector and the video output connector.

Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8" wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 12.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 13 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is less than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt445 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

PC Board Layout Considerations *(continued)*

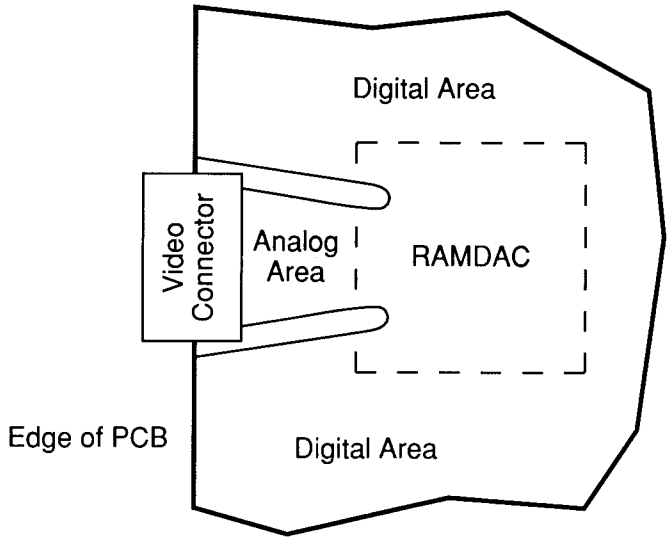


Figure 12. Representative Power/Ground Analog Area Layout

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must have adequate decoupling to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt445 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

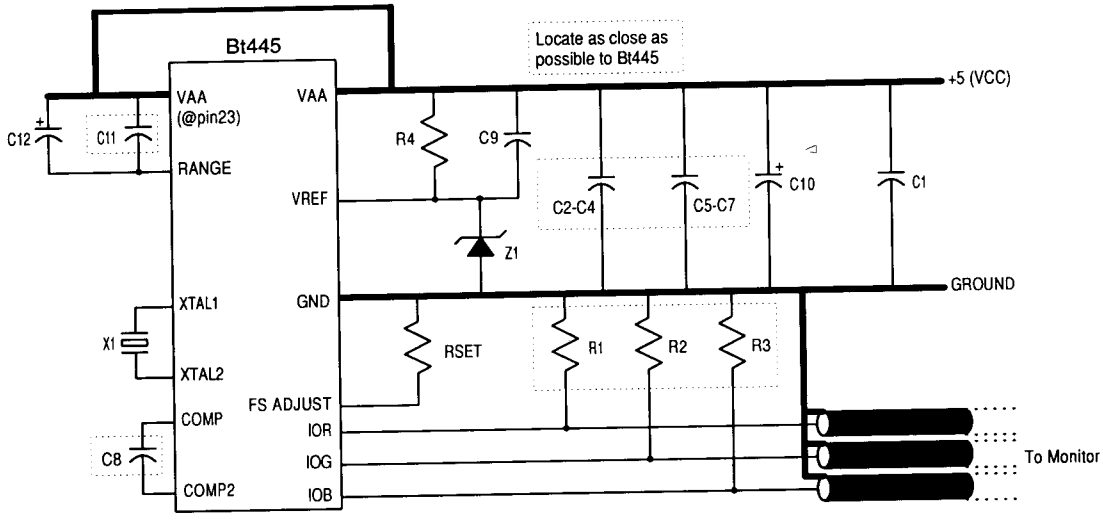
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

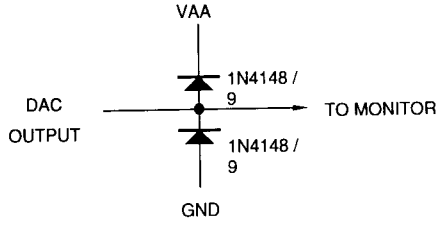
Analog Output Protection

The Bt445 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*





Diode Protection Circuit

Location	Description	Vendor Part Number
C1–C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7, C11	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
C12	4.7 µF tantalum capacitor	tbd
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
X1	20 MHz crystal	tbd
Z1	1.2 Vvoltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt445.

Figure 13. Typical Connection Diagram and Parts List.

Applications Information

Test Features of the Bt445

The Bt445 contains a dedicated test register and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Register

When enabled, the output signature registers operate with the 24 bits of data that are presented to the DAC inputs. These 24-bit vectors represent a single pixel-color, and are presented as inputs simultaneously to the red, green, and blue SARs, as well as the three on-chip DACs.

The SARs act as a wide linear feedback shift register on each succeeding DAC input. It is important to note that in all the multiplexed modes the SARs register every pixel.

The Bt445 will only generate signatures while in active-display (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt445 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 24 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream will be input to the chip, for example, one scan-line or one frame buffer of pixels. Then, at the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay, cursor, and palette bypass data validity is also tested using the signature registers.

It is not simple to describe algorithmically the specific linear feedback shift operation used in the Bt445. The linear feedback configuration are shown in Figure 14.

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel streamfed to the SARs.

When performing system tests that use the signature analysis registers, it is recommended that the pipeline delay be reset prior to the test to provide optimal allowance for input clock drift. This prevents the disruption of pixel data because of pipeline auto-reset, which may occur as the phase relation of the input clock drifts, with respect to the output clocks. Excessive input clock drift may require that signatures be acquired over shorter periods when the maximum drift may be more tightly controlled. This is especially recommended during environmental and power supply variation testing.

Analog Comparator

The other dedicated test structure in the Bt445 is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register. The capture occurs over one LD/SCLKI period set by a logical one at pin P31.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Applications Information *(continued)*

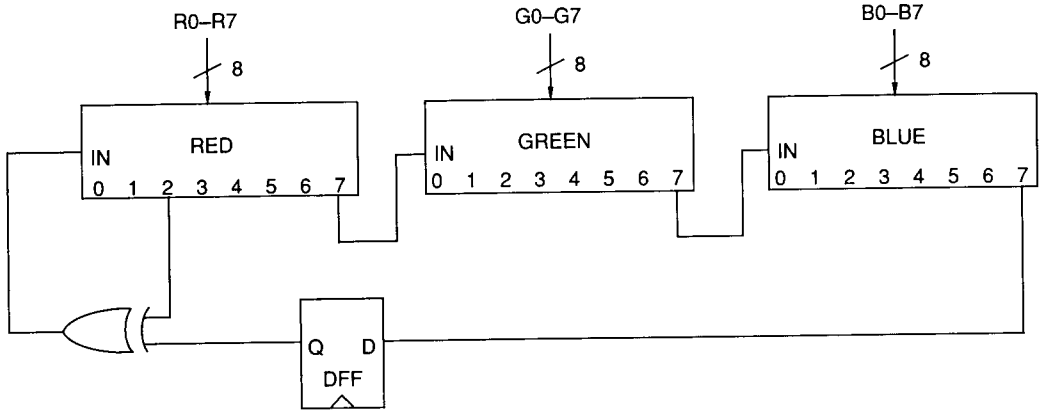


Figure 14. Signature Analysis Register Circuit.

Applications Information *(continued)*

Initializing the Bt445

Following the assertion of the reset signal, the Bt445 pixel unpacking logic and pixel formatting logic are initialized to the Bt458 4:1 MPX mode of operation. See Table 8.

Control Register	Value	Description
Pixel Port Start Position	40	4 pixels, each with 8-bit pseudo color and 2-bit overlay.
Pixel Depth	10	8-bit pseudo color and 2-bit overlay.
Pixel Multiplex Rate	4	4:1 Multiplexed.
Red, Green, Blue Shift	$00	8-bit pseudo-color sources Red, Green, and Blue from same field starting from low-order bit of pixel.
Red, Green, Blue Width	$08	
Red, Green, Blue Enable	$FF	All planes used.
Red, Green, Blue Blink	$00	Pixel blinking disabled.
Overlay Shift	$08	Overlay comes in on next high-order pixels above 8-bit pseudo-color bits.
Overlay Width	2	2-bit overlay supported in Bt458.
Overlay Enable	$03	Bit planes 0 and 1 enabled.
Overlay Blink	$00	Overlay blinking disabled.

Table 8. Reset Initialization.

Applications Information *(continued)*

Color Palette Initialization

Table 9 shows the sequence of MPU writes required to load the color palette entries:

Operation	Description	C(2–0)	Internal Address Register	MPU Data
Color Palette RAM Initialization	Write $00 to address register	000	–	$00
	Write red data to RAM (location $00)	001	$00	$rr
	Write green data to RAM (location $00)	001	$00	$gg
	Write blue data to RAM (location $00)	001	$00	$bb
	Write red data to RAM (location $01)	001	$01	$rr
	Write green data to RAM (location $01)	001	$01	$gg
	Write blue data to RAM (location $01)	010	$01	$bb
	:	:	:	:
	Write red data to RAM (location $FF)	001	$FF	$rr
	Write green data to RAM (location $FF)	001	$FF	$gg
	Write blue data to RAM (location $FF)	001	$FF	$bb
Overlay Color Palette Initialization	Write $00 to address register	000	–	$00
	Write red data to overlay (location $0)	011	$00	$rr
	Write green data to overlay (location $0)	011	$00	$gg
	Write blue data to overlay (location $0)	011	$00	$bb
	Write red data to overlay (location $1)	011	$01	$rr
	Write green data to overlay (location $1)	011	$01	$gg
	Write blue data to overlay (location $1)	011	$01	$bb
	:	:	:	:
	Write red data to overlay (location $F)	011	$0F	$rr
	Write green data to overlay (location $F)	011	$0F	$gg
	Write blue data to overlay (location $F)	011	$0F	$bb
Cursor Palette Initialization	Write $00 to address register	000	–	$00
	Write red data to cursor (location $0)	111	$00	$rr
	Write green data to cursor (location $0)	111	$00	$gg
	Write blue data to cursor (location $0)	111	$00	$bb
	Write red data to cursor (location $1)	111	$01	$rr
	Write green data to cursor (location $1)	111	$01	$gg
	Write blue data to cursor (location $1)	111	$01	$bb
	:	:	:	:
	Write red data to cursor (location $3)	111	$03	$rr
	Write green data to cursor (location $3)	111	$03	$gg
	Write blue data to cursor (location $3)	111	$03	$bb

Table 9. Color Palette Initialization.

Applications Information *(continued)*

Pipeline Delay Initialization

The Bt445 employs a variable pipeline delay to allow for easier system implementation. This scheme allows the LD/SCLKI and VIDCLKI signals to drift relative to the pixel clock (as would occur with varying environmental conditions such as warm-up and power supply fluctuations) without corrupting the output pixel data stream. The amount of allowable drift depends on the MPX Rate; for example, in a 4:1 MPX mode, the drift window is slightly less than 4 pixel clock cycles. This compares favorably with fixed-pipeline delay devices where the drift is necessarily less than one pixel clock to the point of pixel loss or duplication.

For optimum performance, the pipeline depth should be initialized away from the extremes of the drift window to allow for subsequent drift. This is accomplished by the transition of the RESET* signal from 0 to 1 or under the MPU's control by the transition of the RESET PIPELINE field in the Pixel Format Control Register from 0 to 1. The MPU should reset the pipeline whenever any of the following registers or fields are changed: the Pixel Port Start Position Register, the Pixel Unpacking Order Field, the MPX Rate Register, the Pixel Depth Control Register, the PLL Rate Registers, the Pixel Clock PLL Enable Field, The VCO Gain Control Field, or the SCLK* Enable field.

Additionally, when changing any controls affecting the pixel PLL rate or VCO gain, sufficient time should be allowed for the PLL to stabilize to the new rate prior to the MPU issuing the pipeline delay initialization.

Table 10 illustrates the allowable drift windows for LD/SCLKI relative to the pipeline depth initialization time for the various MPX modes.

PLL Initialization

Crystal Frequency Selection

The crystal frequency should be selected based on the required pixel rate(s), the display pixel rate tolerance, and the required system clock outputs. When using the Bt445-generated system clocks, because the system clock ratios are fixed, the crystal reference frequency is usually dictated by required system clock rates. The desired ratio for the PLL can then be computed by dividing required the pixel rate by the crystal frequency, looking up the M and N values in the ratio table for the closest ratio, and ensuring that the display can still satisfactorily operate within the best-fit pixel rate and associated CRT timings.

Ratio Selection

The PLL clock ratio is set by programming the M and N values through the MPU port. Reset M and N values are $18 and $04, respectively, yielding a pixel rate of 5 times the crystal reference.

Table 11 shows the complete range of M/N ratios for M ranges from 25–64 and N ranges from 4–15 and L = 1, for 20.0 and 14.318 MHz crystals.

MPX Rate(s)	Minimum	Maximum	Units
1:1	0	0	Pixel Clocks
2:1	–1	+1	
3:1	–1	+2	
4:1	–2	+2	
5:1	–2	+3	
:	:	:	
63:1	–2	+61	
64:1	–2	+62	

External stopping of the CLOCK and CLOCK* signals is not required for pipeline delay initialization.

Table 10. Allowable LD/SCLKI Drift.

Applications Information *(continued)*

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
3.250	26	8	65.00	N/A	tbd
3.267	49	15	65.33	N/A	tbd
3.273	36	11	65.45	N/A	tbd
3.286	46	14	65.71	N/A	tbd
3.300	33	10	66.00	N/A	tbd
3.308	43	13	66.15	N/A	tbd
3.333	30	9	66.67	N/A	tbd
3.357	47	14	67.14	N/A	tbd
3.364	37	11	67.27	N/A	tbd
3.375	27	8	67.50	N/A	tbd
3.385	44	13	67.69	N/A	tbd
3.400	34	10	68.00	N/A	tbd
3.417	41	12	68.33	N/A	tbd
3.429	48	14	68.57	N/A	tbd
3.444	31	9	68.89	N/A	tbd
3.455	38	11	69.09	N/A	tbd
3.462	45	13	69.23	N/A	tbd
3.467	52	15	69.33	N/A	tbd
3.500	28	8	70.00	N/A	tbd
3.533	53	15	70.67	N/A	tbd
3.538	46	13	70.77	N/A	tbd
3.545	39	11	70.91	N/A	tbd
3.556	32	9	71.11	N/A	tbd
3.571	25	7	71.43	N/A	tbd
3.583	43	12	71.67	N/A	tbd
3.600	36	10	72.00	N/A	tbd
3.615	47	13	72.31	N/A	tbd
3.625	29	8	72.50	N/A	tbd
3.636	40	11	72.73	N/A	tbd
3.643	51	14	72.86	N/A	tbd
3.667	33	9	73.33	N/A	tbd
3.692	48	13	73.85	N/A	tbd
3.700	37	10	74.00	N/A	tbd
3.714	26	7	74.29	N/A	tbd
3.727	41	11	74.55	N/A	tbd
3.733	56	15	74.67	N/A	tbd
3.750	30	8	75.00	N/A	tbd
3.769	49	13	75.38	N/A	tbd
3.778	34	9	75.56	N/A	tbd
3.786	53	14	75.71	N/A	tbd
3.800	38	10	76.00	N/A	tbd
3.818	42	11	76.36	N/A	tbd
3.833	46	12	76.67	N/A	tbd
3.846	50	13	76.92	N/A	tbd
3.857	27	7	77.14	N/A	tbd
3.867	58	15	77.33	N/A	tbd
3.875	31	8	77.50	N/A	tbd
3.889	35	9	77.78	N/A	tbd
3.900	39	10	78.00	N/A	tbd

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
3.909	43	11	78.18	N/A	tbd
3.917	47	12	78.33	N/A	tbd
3.923	51	13	78.46	N/A	tbd
3.929	55	14	78.57	N/A	tbd
3.933	59	15	78.67	N/A	tbd
4.000	28	7	80.00	N/A	tbd
4.067	61	15	81.33	N/A	tbd
4.071	57	14	81.43	N/A	tbd
4.077	53	13	81.54	N/A	tbd
4.083	49	12	81.67	N/A	tbd
4.091	45	11	81.82	N/A	tbd
4.100	41	10	82.00	N/A	tbd
4.111	37	9	82.22	N/A	tbd
4.125	33	8	82.50	N/A	tbd
4.133	62	15	82.67	N/A	tbd
4.143	29	7	82.86	N/A	tbd
4.154	54	13	83.08	N/A	tbd
4.167	25	6	83.33	N/A	tbd
4.182	46	11	83.64	N/A	tbd
4.200	42	10	84.00	N/A	tbd
4.214	59	14	84.29	N/A	tbd
4.222	38	9	84.44	N/A	tbd
4.231	55	13	84.62	N/A	tbd
4.250	34	8	85.00	N/A	tbd
4.267	64	15	85.33	N/A	tbd
4.273	47	11	85.45	N/A	tbd
4.286	30	7	85.71	N/A	tbd
4.300	43	10	86.00	N/A	tbd
4.308	56	13	86.15	N/A	tbd
4.333	26	6	86.67	N/A	tbd
4.357	61	14	87.14	N/A	tbd
4.364	48	11	87.27	N/A	tbd
4.375	35	8	87.50	N/A	tbd
4.385	57	13	87.69	N/A	tbd
4.400	44	10	88.00	N/A	tbd
4.417	53	12	88.33	N/A	tbd
4.429	31	7	88.57	N/A	tbd
4.444	40	9	88.89	N/A	tbd
4.455	49	11	89.09	N/A	tbd
4.462	58	13	89.23	N/A	tbd
4.500	27	6	90.00	N/A	tbd
4.538	59	13	90.77	N/A	tbd
4.545	50	11	90.91	65.08	tbd
4.556	41	9	91.11	65.23	tbd
4.571	32	7	91.43	65.45	tbd
4.583	55	12	91.67	65.62	tbd
4.600	46	10	92.00	65.86	tbd
4.615	60	13	92.31	66.08	tbd
4.625	37	8	92.50	66.22	tbd

Table 11. Sample Pixel Clock Rates.

Applications Information *(continued)*

Reference Frequence:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
4.636	51	11	92.73	66.38	tbd
4.667	28	6	93.33	66.82	tbd
4.692	61	13	93.85	67.19	tbd
4.700	47	10	94.00	67.30	tbd
4.714	33	7	94.29	67.50	tbd
4.727	52	11	94.55	67.69	tbd
4.750	38	8	95.00	68.01	tbd
4.769	62	13	95.38	68.29	tbd
4.778	43	9	95.56	68.41	tbd
4.800	48	10	96.00	68.73	tbd
4.818	53	11	96.36	68.99	tbd
4.833	29	6	96.67	69.20	tbd
4.846	63	13	96.92	69.39	tbd
4.857	34	7	97.14	69.55	tbd
4.875	39	8	97.50	69.80	tbd
4.889	44	9	97.78	70.00	tbd
4.900	49	10	98.00	70.16	tbd
4.909	54	11	98.18	70.29	tbd
4.917	59	12	98.33	70.40	tbd
4.923	64	13	98.46	70.49	tbd
5.000	25	5	100.00	71.59	tbd
5.083	61	12	101.67	72.78	tbd
5.091	56	11	101.82	72.89	tbd
5.100	51	10	102.00	73.02	tbd
5.111	46	9	102.22	73.18	tbd
5.125	41	8	102.50	73.38	tbd
5.143	36	7	102.86	73.64	tbd
5.167	31	6	103.33	73.98	tbd
5.182	57	11	103.64	74.19	tbd
5.200	26	5	104.00	74.45	tbd
5.222	47	9	104.44	74.77	tbd
5.250	42	8	105.00	75.17	tbd
5.273	58	11	105.45	75.50	tbd
5.286	37	7	105.71	75.68	tbd
5.300	53	10	106.00	75.89	tbd
5.333	32	6	106.67	76.36	tbd
5.364	59	11	107.27	76.80	tbd
5.375	43	8	107.50	76.96	tbd
5.400	27	5	108.00	77.32	tbd
5.429	38	7	108.57	77.73	tbd
5.444	49	9	108.89	77.95	tbd
5.455	60	11	109.09	78.10	tbd
5.500	33	6	110.00	78.75	tbd
5.545	61	11	110.91	79.40	tbd
5.556	50	9	111.11	79.55	tbd
5.571	39	7	111.43	79.77	tbd
5.600	28	5	112.00	80.18	tbd
5.625	45	8	112.50	80.54	tbd
5.636	62	11	112.73	80.70	tbd

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
5.667	34	6	113.33	81.14	tbd
5.700	57	10	114.00	81.61	tbd
5.714	40	7	114.29	81.82	tbd
5.727	63	11	114.55	82.00	tbd
5.750	46	8	115.00	82.33	tbd
5.778	52	9	115.56	82.73	tbd
5.800	29	5	116.00	83.05	tbd
5.818	64	11	116.36	83.31	tbd
5.833	35	6	116.67	83.52	tbd
5.857	41	7	117.14	83.86	tbd
5.875	47	8	117.50	84.12	tbd
5.889	53	9	117.78	84.32	tbd
5.900	59	10	118.00	84.48	tbd
6.000	30	5	120.00	85.91	tbd
6.100	61	10	122.00	87.34	tbd
6.111	55	9	122.22	87.50	tbd
6.125	49	8	122.50	87.70	tbd
6.143	43	7	122.86	87.95	tbd
6.167	37	6	123.33	88.30	tbd
6.200	31	5	124.00	88.77	tbd
6.222	56	9	124.44	89.09	tbd
6.250	25	4	125.00	89.49	tbd
6.286	44	7	125.71	90.00	tbd
6.300	63	10	126.00	90.20	tbd
6.333	38	6	126.67	90.68	tbd
6.375	51	8	127.50	91.28	tbd
6.400	32	5	128.00	91.64	tbd
6.429	45	7	128.57	92.05	tbd
6.444	58	9	128.89	92.27	tbd
6.500	26	4	130.00	93.07	tbd
6.556	59	9	131.11	93.86	tbd
6.571	46	7	131.43	94.09	tbd
6.600	33	5	132.00	94.50	tbd
6.625	53	8	132.50	94.86	tbd
6.667	40	6	133.33	95.45	tbd
6.714	47	7	134.29	96.14	tbd
6.750	27	4	N/A	96.65	tbd
6.778	61	9	N/A	97.05	tbd
6.800	34	5	N/A	97.36	tbd
6.833	41	6	N/A	97.84	tbd
6.857	48	7	N/A	98.18	tbd
6.875	55	8	N/A	98.44	tbd
6.889	62	9	N/A	98.64	tbd
7.000	28	4	N/A	100.23	tbd
7.111	64	9	N/A	101.82	tbd
7.125	57	8	N/A	102.02	tbd
7.143	50	7	N/A	102.27	tbd
7.167	43	6	N/A	102.61	tbd
7.200	36	5	N/A	103.09	tbd

Table 11 (continued). Sample Pixel Clock Rates.

Applications Information *(continued)*

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
7.250	29	4	N/A	103.81	tbd
7.286	51	7	N/A	104.32	tbd
7.333	44	6	N/A	105.00	tbd
7.375	59	8	N/A	105.60	tbd
7.400	37	5	N/A	105.95	tbd
7.429	52	7	N/A	106.36	tbd
7.500	30	4	N/A	107.39	tbd
7.571	53	7	N/A	108.41	tbd
7.600	38	5	N/A	108.82	tbd
7.625	61	8	N/A	109.18	tbd
7.667	46	6	N/A	109.77	tbd
7.714	54	7	N/A	110.45	tbd
7.750	31	4	N/A	110.97	tbd
7.800	39	5	N/A	111.68	tbd
7.833	47	6	N/A	112.16	tbd
7.857	55	7	N/A	112.50	tbd
7.875	63	8	N/A	112.76	tbd
8.000	32	4	N/A	114.55	tbd
8.143	57	7	N/A	116.59	tbd
8.167	49	6	N/A	116.93	tbd
8.200	41	5	N/A	117.41	tbd

Reference Frequency:			20.0	14.31818	
M/N	*M*	*N*	*PCLK*	*PCLK*	*VCO*
8.250	33	4	N/A	118.12	tbd
8.286	58	7	N/A	118.64	tbd
8.333	50	6	N/A	119.32	tbd
8.400	42	5	N/A	120.27	tbd
8.429	59	7	N/A	120.68	tbd
8.500	34	4	N/A	121.70	tbd
8.571	60	7	N/A	122.73	tbd
8.600	43	5	N/A	123.14	tbd
8.667	52	6	N/A	124.09	tbd
8.714	61	7	N/A	124.77	tbd
8.750	35	4	N/A	125.28	tbd
8.800	44	5	N/A	126.00	tbd
8.833	53	6	N/A	126.48	tbd
8.857	62	7	N/A	126.82	tbd
9.000	36	4	N/A	128.86	tbd
9.143	64	7	N/A	130.91	tbd
9.167	55	6	N/A	131.25	tbd
9.200	46	5	N/A	131.73	tbd
9.250	37	4	N/A	132.44	tbd
9.333	56	6	N/A	133.64	tbd
9.400	47	5	N/A	134.59	tbd

Table 11 (continued). Sample Pixel Clock Rates.

Note: All Pixel Clock frequencies shown are prior to the "L" divider section. All of the listed frequencies may be divided by 1, 2, 4, or 8 to provide lower pixel clock rates.

Frame Buffer Interface Configurations

The Bt445 may be operated with an internal PLL or an external clock generator. Additionally, the Bt445 may be used to generate the VRAM serial shift clock signal, or this signal may be generated externally. The following figures show examples of the frame buffer interface when using the Bt445 in various modes.

Externally Generated Pixel Clock with Externally Generated VRAM Serial Shift Clock

In this configuration, neither the SCLK* nor VIDCLK* outputs of the Bt445 are used, and thus they should be disabled via the command registers. The pixel clock, load clock, and VRAM serial shift clock are externally generated by a device such as the Bt438 or Bt440. Figure 15 illustrates this configuration.

The multiplex rates supported are limited by the modes for which the external clock divider (i.e., the Bt440 in this case) can be configured. The SYNC* and BLANK* information loaded correspond to the pixel data loaded on the same LD clock rising edge. The maximum pixel clock rate is 150 MHz.

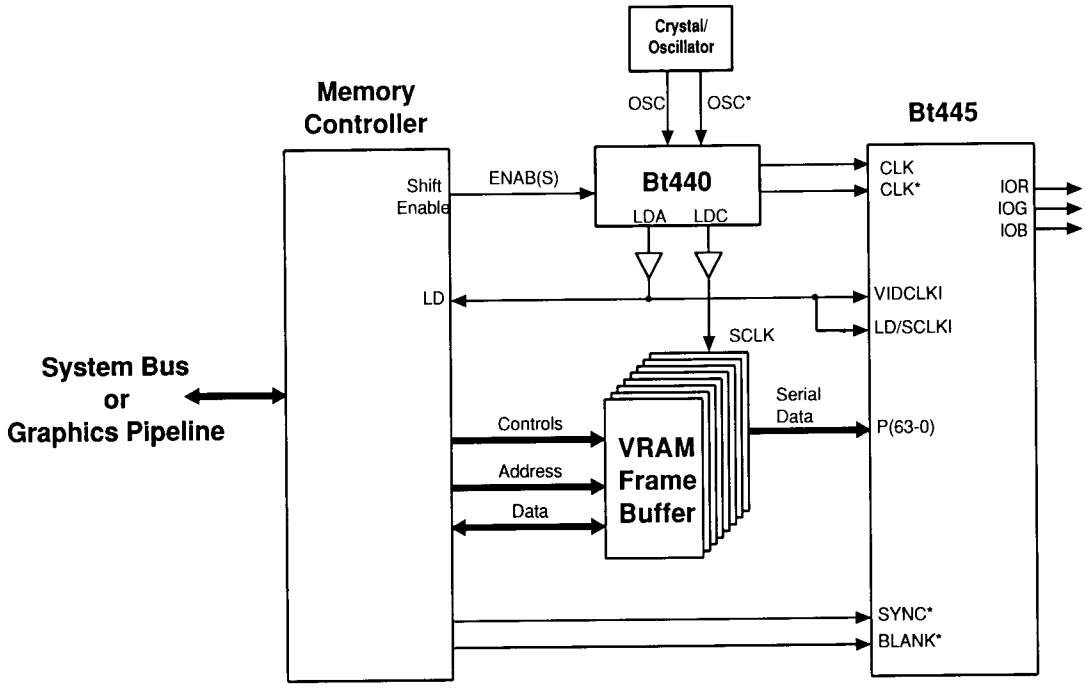


Figure 15. Frame Buffer Interface, External Pixel Clock, and Serial Clock Generation.

Applications Information *(continued)*

PLL-Generated Pixel Clock with Externally Generated VRAM Shift Clock

In this configuration, the Bt445 generates the pixel clock internally from the M and N values contained in the control registers. The VRAM shift clock is still externally generated, but the system must use the Bt445's VIDCLK* output, as there is no other system reference that is phase related to the pixel clock. The memory controller produces a clock gate signal for generating the VRAM shift clock from VIDCLK*. Figure 16 illustrates this configuration.

The inverting drivers used to generate LD/SCLKI and the VRAM shift clock should ideally have correlated delays and high-impedance, low capacitance inputs.

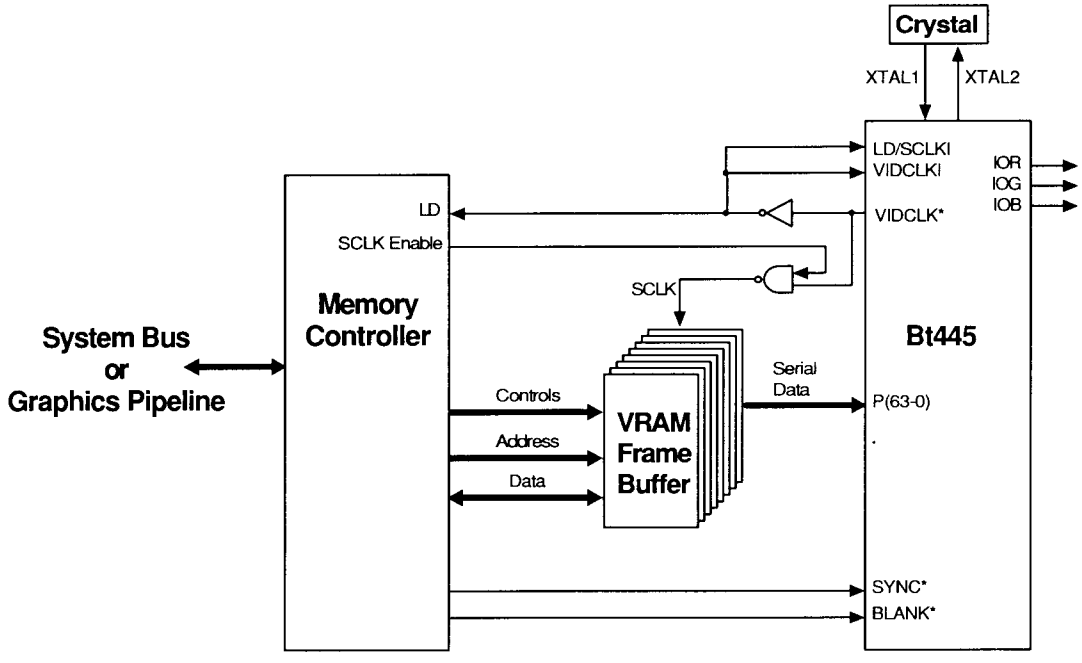


Figure 16. Frame Buffer Interface, with PLL Pixel Clock and no Bt445-Provided Shift Clock.

Bt445-Generated VRAM Shift Clock, Externally-Generated Pixel Clock

In this configuration, the pixel clock is generated in an external oscillator. The Bt445 provides two clocks to the system: VIDCLK* and SCLK*. VIDCLK* is always free running and is used to control the CRT timing generator, usually part of the controller. VIDCLKI is used to register the SYNC*, and BLANK* signals. LD/SCLKI is used to register the pixel data. Figure 17 illustrates this configuration.

SCLK* is asserted as needed to shift out pixel data from the VRAMs, according to the MPX rate specified by a control register. Generally, VIDCLK* and SCLK* do not run at the same rate; hence, the granularity with which SYNC* and BLANK* are specified is not the same as the MPX rate. As a result, the last group of pixels loaded with LD/SCLKI at the end of an active scan line, may not all be displayed. It should be noted that in this configuration, the SYNC* and BLANK* information does not correlate to the data on the Bt445's pixel input port; however, the Bt445 internally aligns the CRT timing controls with the pixel data for output. Also, the buffer delays for VIDCLK* and SCLK* need not be correlated.

The SCLK control signal supplied by the memory controller is used only to insert shift clocks for the purpose of loading the shift register tap address required by VRAMs supporting split-shift register operations.

The pixel rate in this configuration may be up to 150 MHz.

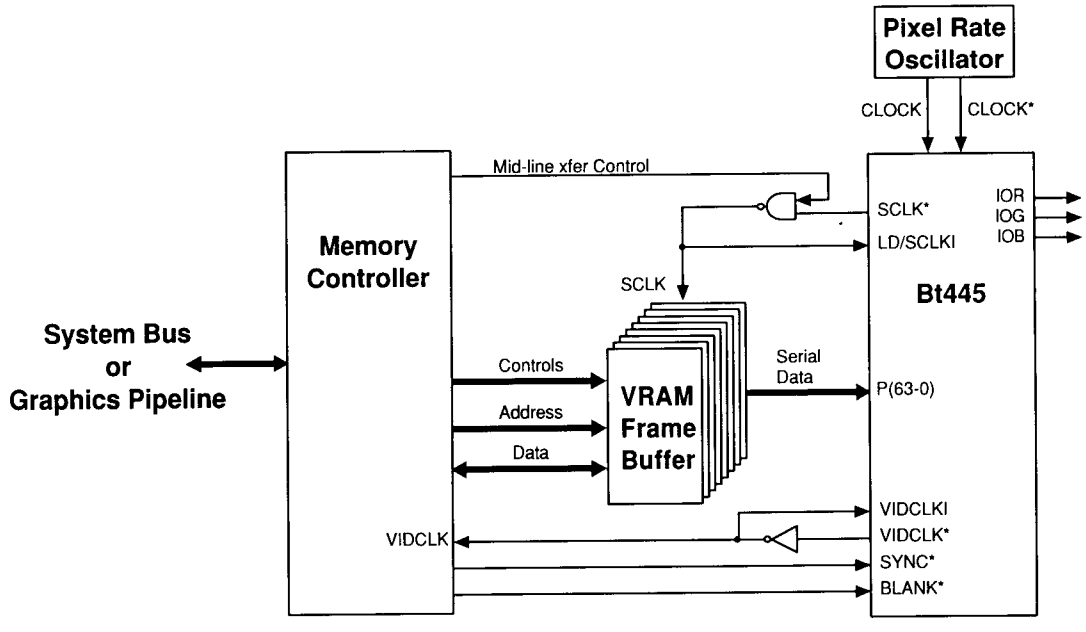


Figure 17. Frame Buffer Interface with Externally Generated Pixel Clock and Bt445-Generated SCLK.

Applications Information *(continued)*

The Bt445-Generated VRAM Shift Clock and PLL-Generated Pixel Clock

This configuration is very similiar to the previous one without the PLL generated pixel clock. Here, a relatively low frequency crystal is connected to the OSC, OSC* inputs, instead of using an ECL oscillator operated on a pseudo-ECL supply (i.e., +5 and GND) connected to the CLOCK and CLOCK* inputs of the Bt445.

In this configuration, the maximum pixel rate is limited by the PLL maximum operational frequency of 135 MHz. See Figure 18.

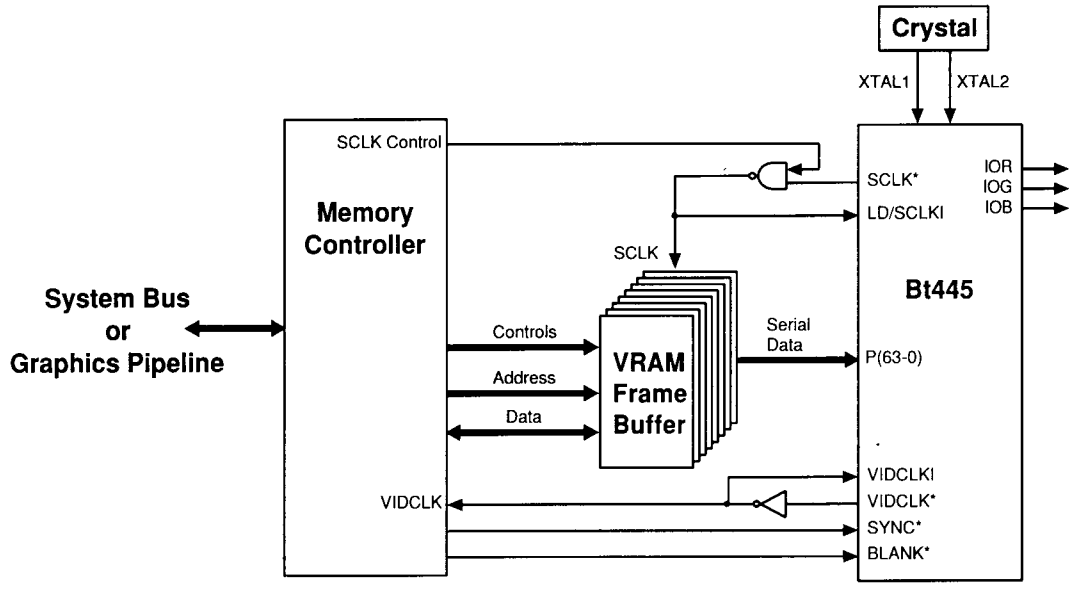


Figure 18. Frame Buffer Interface for Bt445-Generated VRAM Serial Clock and Pixel Clock.

Applications Information *(continued)*

Digital Output Port

Figure 19 shows a simplified typical connection between the Bt445, a CRT display, and a typical VGA resolution TFT flat-panel display. The VSYNC* and HSYNC* inputs to the Bt445 are not internally used; they are only synchronized with the pixel data and presented on the PVSYNC* and PHSYNC* outputs, respectively. This allows for variations between CRT and flat-panel SYNC signal timings and durations. However, the horizontal line rates and pixel rates must be identical if both displays are to be driven simultaneously.

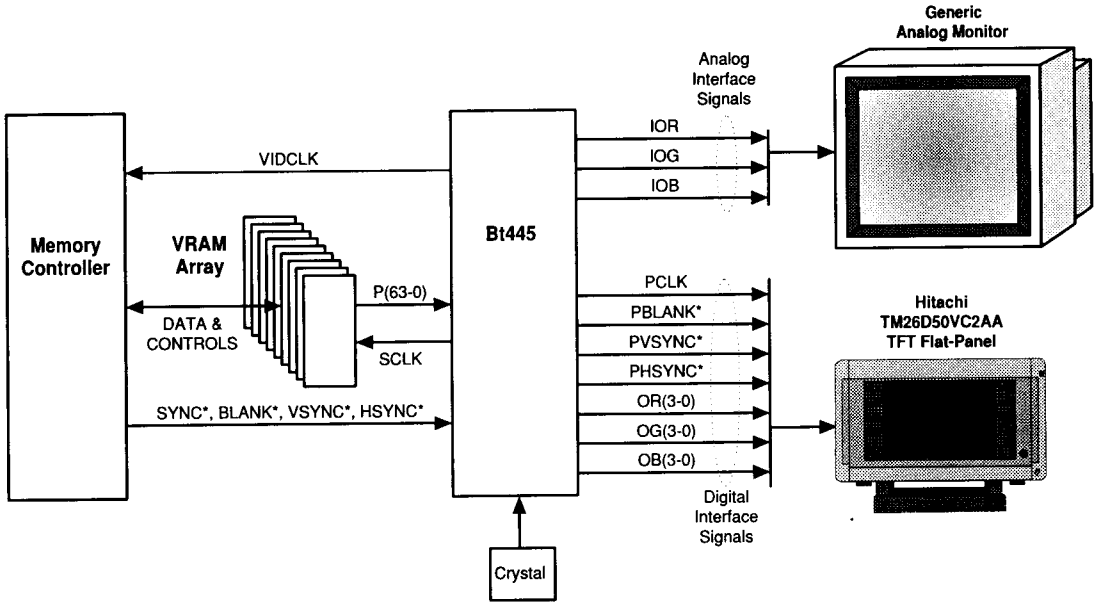


Figure 19. Typical Connection Diagram for Digital Output Port to 640 x 480 TFT Flat-Panel Display.

Applications Information *(continued)*

Interfacing to High-Resolution Flat-Panel Displays

Preliminary information suggests that high-resolution flat-panel displays will achieve the required pixel rates without using excessive clock speeds if more than 1 pixel per clock cycle is provided, in the same fashion that high-resolution Brooktree RAMDACs accept pixels at the input pixel port. The Bt445's digital output port may operate up to 55 MHz, providing the bandwidth required, for example, for a 1024 x 768 active matrix panel. However, to provide 2 pixels at half the clock rate, some intervening logic may be used. Refer to Figure 20.

For proper operation, the control signals PBLANK*, PVSYNC*, and PHSYNC* should only change on an even pixel. The sample logic shown resets the generated clock and pixel data on each edge of PBLANK*. Also note that the clock-to-Q delay on the flip-flop, which generates LD Clock to the panel, should be faster than the clock-to-Q delay of the pixel data registers.

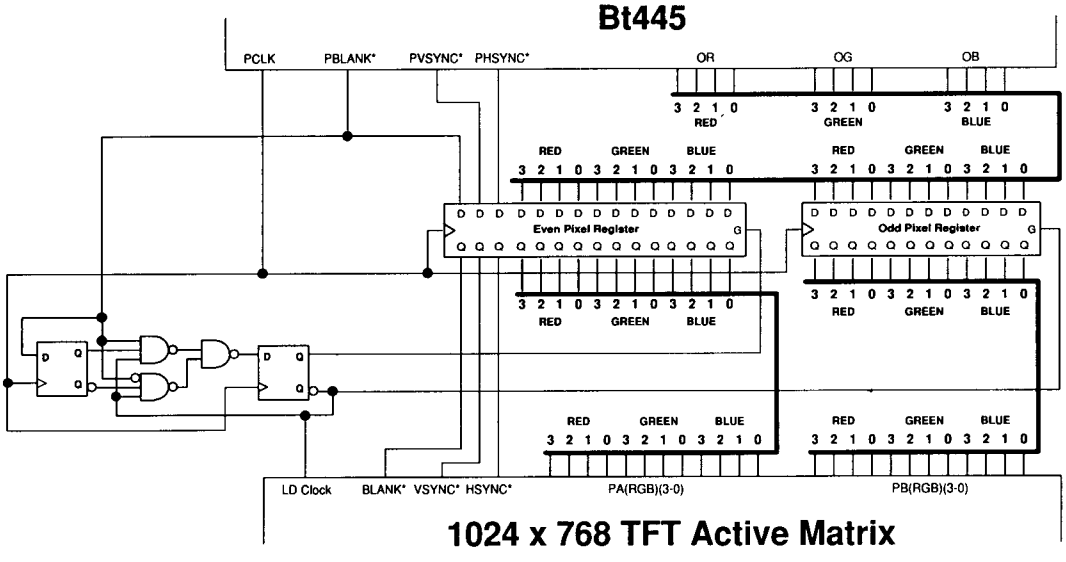


Figure 20. Interfacing the Bt445 with a 1024 x 768 TFT Active Matrix Flat Panel.

Applications Information *(continued)*

Digital Output Connection in 8-8-8 True-Color Mode

Figure 21 shows a simplified typical connection diagram using 8-8-8 true-color mode, to a Bt858 video encoder.

The registers are used to hold the data presented in the first half of the PCLK cycle; data presented during the second half of the PCLK cycle is held in the transparent latches, which are open during the clock high level. The configuration shown assumes that the external CRT timing generator provides the appropriate SYNC* and BLANK* signals at the input of the Bt445 for running the Bt858 in master mode 0. The PCLK may need to be re-driven and/or delayed to minimize PCLK loading and to meet hold time requirements of the Bt858.

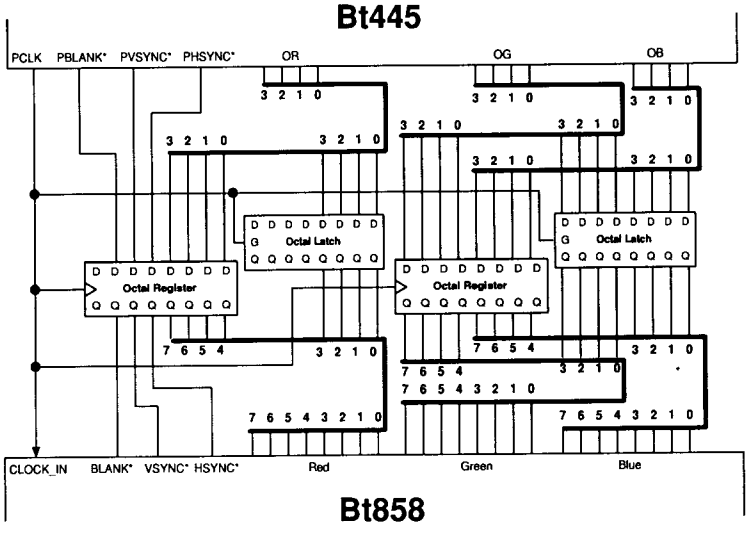


Figure 21. Interfacing the Bt445 to the Bt858.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω
Junction Temperature	Tjmax			+125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55			°C
Storage Temperature	TS	–65		+125	°C
Junction Temperature	TJ			+150	
Ceramic Package					°C
Plastic Package				+175	°C
				+150	
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL				°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS device on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*, VIDCLKI, and LD/SCLKI)					
Input High Voltage	VIH	2.0		VAA+0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Digital Inputs with Internal Pullups (Pixel Inputs and JTAG Pins)					
Input High Voltage	VIH	2.0		VAA+0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			60	µA
Input Low Current (Vin = 0.4 V)	IIL			–60	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Pixel Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA–1.0		VAA+0.5	V
Input Low Voltage	VKIL	GND–0.5		VAA-1.6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Clock Inputs (VIDCLKI, LD/SCLKI)					
Positive going threshold	VT+		1.7		V
Negative going threshold	VT–		0.9		V
Hysteresis	(V_{T+}–V_{T-})		0.8		V
Input High Current (Vin = 2.4 V)	Iih			1	µA
Input Low Current (Vin = 0.4 V)	Iil			–1	µA
Input Capacitance (f=1 MHz, Vin = 4.0 V)	Cin		4	10	pF
Digital Outputs (except D(7–0), PCLK, VIDCLK*, SCLK*)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			10	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			10	pF

See test conditions on the next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs with Internal Pullups (except D(7–0), VIDCLK*, SCLK*)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			60	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			10	pF
Digital Outputs (VIDCLK*, SCLK*)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			10	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			20	pF
Digital Outputs (PCLK)					
Output High Current (Voh=2.4 V)	Ioh			1	mA
Output Low Current (Vol=0.4 V)	Iol			1	mA
Three-state Current	Ioz			60	µA
Load Capacitance (includes board wiring and capacitance at buffer input)	Cl			20	pF
Digital Outputs (D(7–0))					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
Three-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC- to-DAC Matching			2	5	%
Output Compliance	VOC	–1.0		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % VAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

AC Characteristics

Input Clock

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			150			135			110	MHz
Clock Cycle Time	12	6.7			7.4			9.09			ns
Clock Pulse Width High	13	2.7			3			4			ns
Clock Pulse Width Low	14	2.7			3			4			ns

MPU Port

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
R/W, C0, C1 Setup	1	0			0			0			ns
R/W, C0, C1 Hold	2	15			15			15			ns
CE* Low Time	3	50			50			50			ns
CE* High Time	4	25			25			25			ns
CE* ↓ to Data Driven	5	7			7			7			ns
CE* ↓ to Data Valid	6			75			75			75	ns
CE* ↑ to Data Three-Stated	7			15			15			15	ns
Write Data Setup Time	8 (Note 1)	35			35			35			ns
Write Data Hold Time	9	3			3			3			ns

Note 1: The parameter shown guarantees write data capture. To prevent unnecessary pixel disturbances when writing control registers, the write data should be valid throughout the CE* active duration.

Input Pixel

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LD/SCLKI	LDmax			75			75			75	MHz
Pixel and Control Setup	10	3			3			3			ns
Pixel and Control Hold	11	2			2			2			ns

AC Characteristics *(continued)*

VIDCLKI

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
VIDCLKI Cycle Time	15	13.3			13.3			13.3			ns
VIDCLKI Pulse Width High	16	5.32			5.32			5.32			ns
VIDCLKI Pulse Width Low	17	5.32			5.32			5.32			ns
BLANK*, HSYNC*/SYNC*, VSYNC* Setup											
BLANK*, HSYNC*/SYNC*, VSYNC* Hold											

Analog Output

Parameter	Symbol	150 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog Output Delay	18		TBD			TBD			20		ns
Analog Output Rise/Fall	19		2			2			2		ns
Analog Output Settling (Note 1)	20			8			8			8	ns
TTL Output Skew	21			TBD			TBD			TBD	ns
Clock/Data Feedthrough (Note 2)			35			35			35		pV–sec
Glitch Impulse (Note 3)			50			50			50		pV–sec
Analog Output Skew (Note 4)			0	2		0	2		0	2	ns
Pipeline Delay		TBD		TBD	TBD		TBD	6		10	Clocks
VAA Supply Current (Note 5)	IAA			TBD			TBD			TBD	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10 percent and 90 percent points. ECL input values are VAA – 0.8 to VAA – 1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20 percent and 80 percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 40 pF. See timing notes in Figures 22–26. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Note 1: Output settling time measured from 50 percent point of full-scale transition to output settling within ±1 LSB.

Note 2: Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74 HC logic. Settling time does not include clock and data feedthrough.

Note 3: Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

Note 4: Output delay time measured from 50 percent point of the rising clock edge to 50 percent point of full-scale transition.

Note 5: At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20°C. IAA (max) at VAA = 5.25 V, TA = 0°C.

AC Characteristics *(continued)*

System Clock Generation AC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
VAA valid to VIDCLK stable				tbd	ns
VAA valid to CPUCLK stable				tbd	ns
VAA valid to MCLK stable				tbd	ns
RESET* active pulse width	33	tbd			ns
S0, S1 to RESET* setup time	34			tbd	ns
S0, S1 to RESET* hold time	35			tbd	ns
CE* rise to new VIDCLK rate	36	tbd		tbd	ns
CE* rise to new CPUCLK rate	37	tbd		tbd	ns
S0, S1 to new CPUCLK rate	38			tbd	ns
RESET* to new CPUCLK rate	39			tbd	ns
CPUCLK	Fmax			50	MHz
MCLK20	Fmax			20	MHz
MCLK25	Fmax			25	MHz
CPUCLK, MCLK20, MCLK25 rise/fall time				5	ns
CPUCLK, MCLK20, MCLK25 duty cycle		40	50	60	%
CPUCLK, MCLK20, MCLK25 Jitter				tbd	

PLL Clock Generation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Crystal/Oscillator Frequency		6	20	25	MHz
PLL Clock Generator Multiplicand	M	25		63	
PLL Clock Generator Divisor	N	4		15	
PLL M/N Ratio		tbd		tbd	
PLL M/N Generated Pixel Clock Rate		65		135	MHz
PLL M/N Generated Pixel Clock Accuracy		tbd		tbd	%
PLL M/N Generated Pixel Clock Jitter				tbd	

Above parameters apply to predivided (i.e., before applying 1/L) pixel clock generation.

AC Characteristics *(continued)*

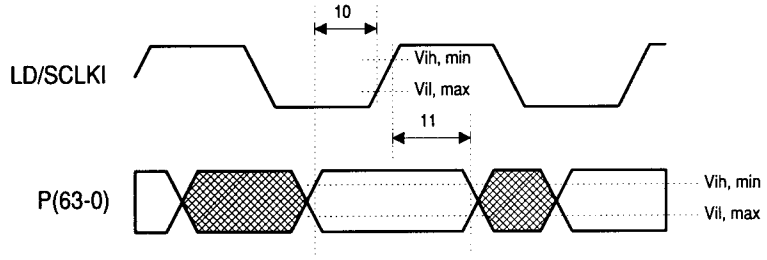


Figure 22. Input Pixel Timing.

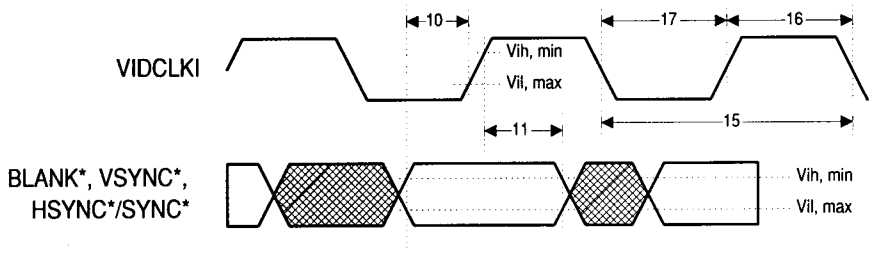


Figure 23. Input Control Timing.

AC Characteristics *(continued)*

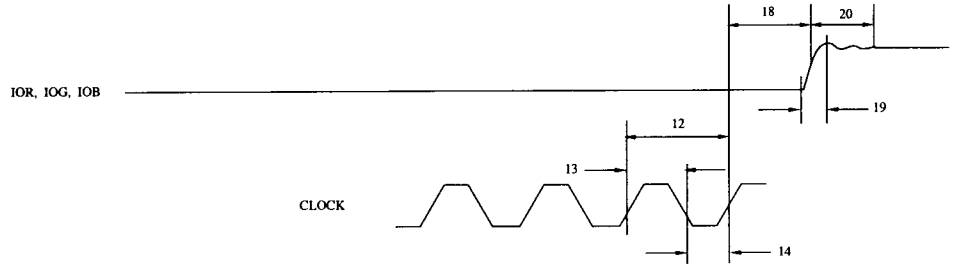


Figure 24. Video Output Timing.

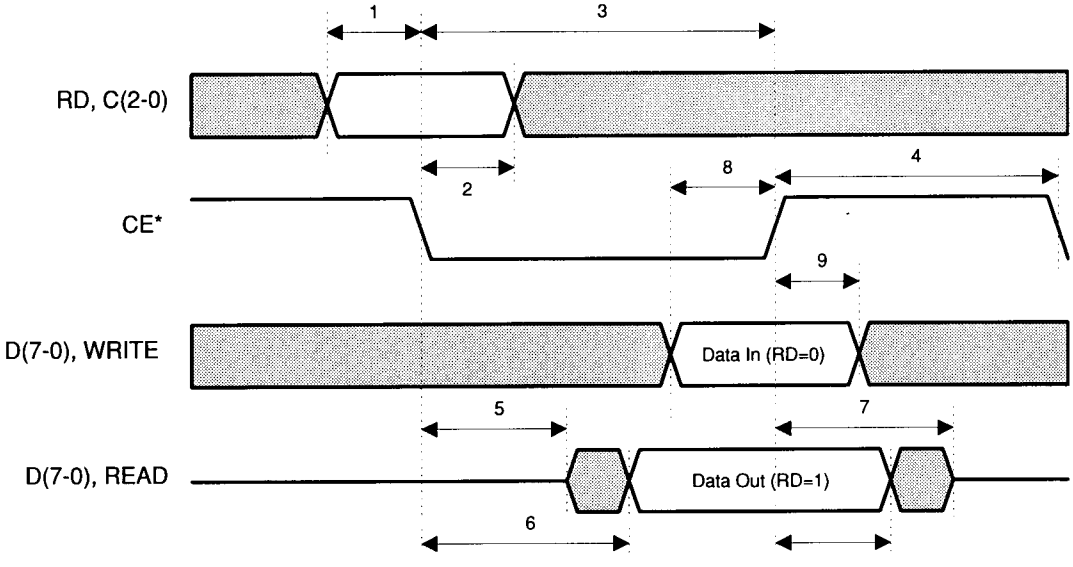


Figure 25. MPU Read/Write Timing.

AC Characteristics *(continued)*

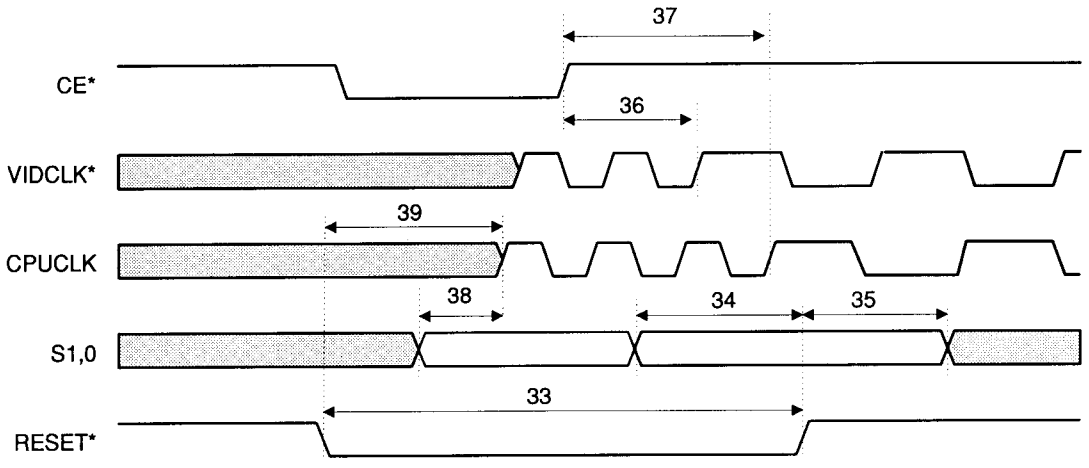


Figure 26. Reset, CPU Clock, and VIDCLK* Output Timing.

AC Characteristics *(continued)*

Digital Pixel Output Port AC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
PCLK Cycle Time (Note 1) 4-4-4 Mode 8-8-8 Mode	40	 18.2 36.4			ns
PCLK Edge to Data, Control Delay	41			15	ns
PCLK Edge to Data, Control Hold	42	10			ns
PCLK Pulse High Duty Cycle	43	40		60	%
PCLK VIDCLK*, SCLK* rise/fall time			3		ns
PSYNC*, PBLANK*, PVSYNC*, PHSYNC* rise/fall time			7		ns
O(R,G,B)(3–0) cycle time		36.4			ns
O(R,G,B)(3–0) rise/fall time			5		ns

Note 1: The cycle time parameters apply only when the PCLK output is enabled. See Figure 27.

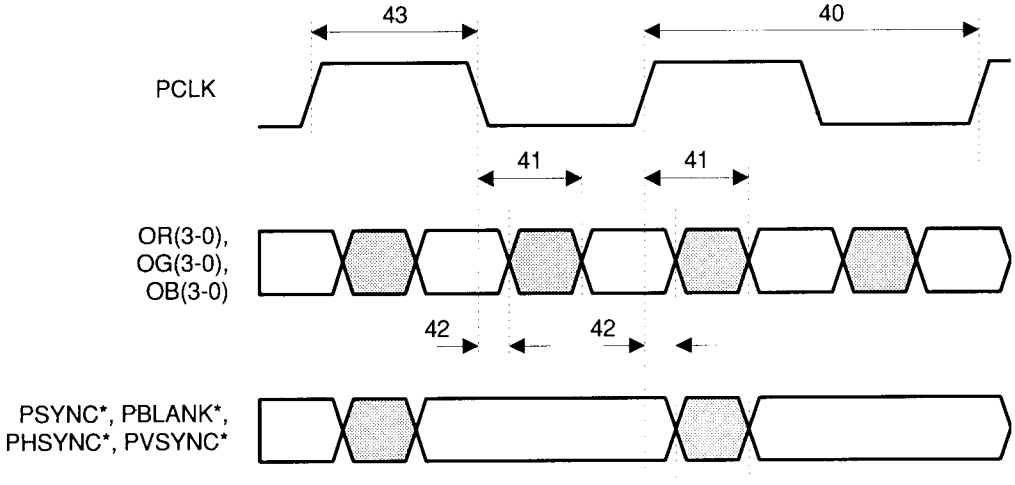


Figure 27. Pixel Output Port Timings.

Ordering Information

Model Number	Speed (MHz)	Package	Ambient Temperature Range
Bt445KPF150	150	160-pin Plastic Quad Flatpack	0° to +70° C
Bt445KPF135	135	160-pin Plastic Quad Flatpack	0° to +70° C
Bt445KPF110	110	160-pin Plastic Quad Flatpack	0° to +70° C